Application Note for Molded Plastic QFN Packages

Monolithic Packaged Microwave IC

1. General considerations on plastic molded packages

SMD* packaged MMIC are now massively adopted for microwave and millimeter-wave applications. The use of such packages requires some specific knowledge in order to optimize the performances. In particular, the design of the motherboard has a strong impact on the overall performance since transition from the package leads to the transmission lines can lead to strong parasitic effects.

The UMS RoHS* compliant plastic QFN* packages, SMT* compatible are appreciated for their very good electrical and thermal performances at low cost. Thanks to a limited area and very short leads, they perfectly suit to the microwave circuits where the package’s parasitic elements must be as small as possible in order to be negligible at high frequency. A lead to lead pitch of 0.5mm gives the best trade-off between electrical performances and industrial constraints up-to 40GHz. The performances of the packaged products are optimum when the effects of the package are taken into account during the design of the MMIC*.

The lead-frame structure made of copper (C194 alloy) includes small leads but also a large metallic exposed-pad acting as an efficient ground-pad and a thermal drain to the PCB* circuit. So, the thermal and electrical ground paths are optimum, and the embedded MMIC is working in very good conditions (see Figure 1).

* See Glossary
Packages are LASER marked on top-side as shown on the Figure 1. The package top marking includes a Pin#1 index and three lines of text used for the device identification.

- Line 1: UMS logo.
- Line 2: device part number.
- Line 3: date code
  - YY stands for the two last digits of the assembly year.
  - WW stands for the week in the assembly year (from 01 to 52).
  - ZZ are two optional characters used internally at UMS for lot identification.

**Remark:** In some cases, samples or prototypes can be marked with white ink.

The mold protection of the plastic QFN acts as a very good mechanical protection for SMT handling steps.

A product qualification must include a set of environmental and ageing tests [4].

The UMS’s QFN plastic packages are compliant with RoHS directive (Pb* free). The list of the materials constituting the product is given on the Figure 2.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Material</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MMIC</td>
<td>GaAs</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Die attach</td>
<td>Epoxy resin with silver filler</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Bonding Wire</td>
<td>Gold</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Frame</td>
<td>Copper (C104) with Sn external finish</td>
<td>Sn finish on back side, see 4a</td>
</tr>
<tr>
<td>4a</td>
<td>Frame external Sn finish</td>
<td>Matte tin (Sn), thickness 400 micron</td>
<td>Package’s exposed surfaces only</td>
</tr>
<tr>
<td>5</td>
<td>Lead</td>
<td>Copper (C104) with Sn external finish</td>
<td>Sn finish on back side, see 5a Ag finish on top side, see 5b</td>
</tr>
<tr>
<td>5a</td>
<td>Lead external Sn finish</td>
<td>Matte tin (Sn), thickness 400 micron</td>
<td>Package’s exposed surfaces only</td>
</tr>
<tr>
<td>5b</td>
<td>Lead bond pad Ag finish</td>
<td>Silver spots (Ag), thickness &lt;40 pinch max</td>
<td>Lead’s internal bond area</td>
</tr>
<tr>
<td>6</td>
<td>Mold Resin</td>
<td>Multi-Aromatic Resin (Br/Se free)</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2:** Example of QFN products build-up structure.
Some UMS QFNs are also available with a NiPdAu treatment of the bottom contacts and remain compatible with the RoHS SMT assembly processes on PCB.

The QFN devices are designed to be mounted onto any standard PCB compatible with SMT process. But, of course at millimetre-wave frequencies a special care must be taken at the PCB level to manage a good electrical and thermal matching of the device. This application note gives guide lines and recommendations in order to design the appropriate motherboard and take advantage of the best circuit performances. Further information can be available under request. However, UMS reminds that the customer is responsible of the development of their PCB.

2. UMS’s QFN packages outlines

Considering the specificities of the microwave products and the impact of the package on the device performances, UMS proposes several dimensions of over-molded plastic packages in order to match perfectly with the specificities of each MMIC. This family of packages complies with high performances and takes advantage of the standard low cost assembly solutions available today for mass production.

The table below gives some available QFN sizes at UMS:

<table>
<thead>
<tr>
<th>Package case</th>
<th>UMS designation</th>
<th>Package Outlines</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 3x3, 16 leads</td>
<td>QAG</td>
<td>See annex 6.1</td>
</tr>
<tr>
<td>QFN 3x3, 16 leads, 2RF fused leads</td>
<td>QAG</td>
<td>See annex 6.2</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads</td>
<td>QDG</td>
<td>See annex 6.3</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads, 2RF fused leads</td>
<td>QDG</td>
<td>See annex 6.4</td>
</tr>
<tr>
<td>QFN 4x5, 24 leads</td>
<td>QEG</td>
<td>See annex 6.5</td>
</tr>
<tr>
<td>QFN 5x5, 32 leads</td>
<td>QFG</td>
<td>See annex 6.6</td>
</tr>
<tr>
<td>QFN 5x6, 36 leads</td>
<td>QXG</td>
<td>See annex 6.7</td>
</tr>
<tr>
<td>QFN 6x6, 40 leads</td>
<td>QJG</td>
<td>See annex 6.8</td>
</tr>
</tbody>
</table>

The package outlines have been defined based on the JEDEC MO-220 standard [1].
3. PCB design

This paragraph presents some recommendations shared by UMS to design the PCB. The development of the PCB must be a point of attention for the functionality of an enhanced motherboard, nevertheless this development strongly depends on each customer’s solution and UMS doesn’t propose a standard.

3.1. General considerations for PCB design

The products developed by UMS are tested on an evaluation board in order to guarantee the best performances at the customer level in the equipment. Since the internal design of the MMIC is generally based on a micro-strip structure, the motherboard where the QFN device will be mounted should be designed in accordance with this configuration. Indeed, the motherboard acts as a:

**Signal feeding structure to the QFN device:** Transmission lines are needed on the PCB. For electromagnetic reasons, a micro-strip mode is generally chosen and helps to avoid parasitic propagations modes on the PCB. It will also help to minimize the electrical transmission losses. The UMS’ QFN packages are generally designed to be matched on 50Ω loads. However, the motherboard in the close area around the QFN device should be designed to have a good impedance transition from the micro-strip line to the package leads.

**The main electrical grounding of the QFN:** Since the QFN device at millimeter-wave frequencies contains generally a micro-strip chip, it is necessary to provide a very good grounding of the package to the PCB’s ground. The main ground interface between the package and the motherboard is done through the package exposed pad (see Figure 1) which is soldered to the PCB’s ground pad (see Figure 3) in the case of a SMT mounting process. The link between the ground of the sub-system and the ground pad on the motherboard is generally done using a metallic via-hole structure. A very standard configuration with metallic via holes to connect the sub-system ground at the PCB’s back-side interface to the package exposed pad is presented Figure 4.
**The main heat-sink of the QFN:** The QFN package thanks to its copper lead-frame has very good thermal performances. The dissipated power is easily spread out from the package through the exposed pad to the PCB. Via holes in the PCB will act as thermal drain to dissipated the thermal energy to the main heat-spreader of the sub-system (see Figure 4).

![Figure 3: General overview of a QFN motherboard.](image1)

![Figure 4: Cross section view of a QFN device assembled on a PCB.](image2)

**3.2. Typical UMS evaluation boards**

SMD type packages from UMS allow the design and fabrication of mm-wave modules at low cost. Therefore, a suitable motherboard environment was chosen according to this aim. All tests and verifications were performed on Rogers RO4003. This material has a permittivity of 3.38 and is used with a thickness of 203µm [8mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line should have a strip width of about 460µm [approximately 18mils]. Other materials with similar properties can be used as well.
The product datasheet generally includes the recommended motherboard used for the product characterization. Sometimes, for different products with a same package size, slight differences can be observed between the motherboard proposed in the datasheet. These differences might come from product specificities.

It is recommended to use as much as possible the proposed layout and technology shown in the product’s datasheet in order to achieve the best performances out of the packaged product.

### 3.2.1. Recommended package footprint on PCB

The QFN packages outline drawings can be provided as DXF CAD files on request in order to help to design the PCB footprint.

Most of the electrical tests done at UMS are performed on a demonstration board with a grid of plated via-holes through the substrate with a diameter of less than 300µm [12mils] and a spacing lower than 700µm [28mils] from the centres of two adjacent via holes. Via holes grid should cover the whole area of the ground pad.

In order to improve the impedance matching, the nearest via holes to the RF ports should be as close as possible from the edges of the PCB ground pad which should be shaped as a CPW structure (ground / signal / ground) surrounding the RF port (see Figure 6).

Since via holes are also important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between the package and the heat sink. However, it is important to consider that via holes internal copper plating will always act as the main thermal drain.

Via filling is also recommended for SMT assembly reasons. Conductive epoxy or any other appropriate thermal conductive material can be used before solder past deposition in order to avoid solder wicking into via holes during the reflow process. This configuration will help to decrease the thermal resistance of the PCB structure, but it will also avoid low package stand-off height.

For the power devices, the use of heat slugs in the motherboard instead of a grid of via holes is recommended.
The table hereafter gives the via holes geometry for some examples of QFN package size.

<table>
<thead>
<tr>
<th>Via-hole external diameter (mm)</th>
<th>OAG QFN 3x3 16L</th>
<th>OAG QFN 3x3 16L 2RF fused lead</th>
<th>QDG QFN 4x4 24L</th>
<th>QDG QFN 4x4 24L 4RF fused lead</th>
<th>QEG QFN 4x5 (or 5x4) 24L</th>
<th>QFG QFN 5x5 32L</th>
<th>QXG QFN 5x6 36L</th>
<th>QJG QFN 6x6 40L</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Via-hole internal diameter (mm)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Number of vias under the package</td>
<td>9</td>
<td>9</td>
<td>16</td>
<td>16</td>
<td>30</td>
<td>36</td>
<td>42</td>
<td>49</td>
</tr>
<tr>
<td>Via holes pitch (mm)</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
<td>0.60</td>
</tr>
<tr>
<td>Via holes height (=PCB thickness) (mm)</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
</tr>
<tr>
<td>Rth_PCB_UMS: Estimated thermal resistance equivalent to the package footprint on PCB (°C/W)</td>
<td>1.46</td>
<td>1.46</td>
<td>0.82</td>
<td>0.82</td>
<td>0.44</td>
<td>0.36</td>
<td>0.31</td>
<td>0.27</td>
</tr>
</tbody>
</table>

### 3.3. Recommendations for PCB design adjustments

Several parameters may influence the design of mother board required for the application as:

- the PCB stack-up structure
- the PCB materials properties
- the PCB thermal capacitance
- the PCB patterns resolution
- the solder paste properties
- the fabrication tolerances of the stencil printer
- the pick & place equipment placement accuracy
- the reflow process

Since it is not possible to define a generic motherboard layout fully compatible with all the industrial SMT processes, this paragraph intent to provide some guides line to adjust the PCB design for a better adaptation to the selected SMT process. But the recommendation given here after should not replace the design rules provided by the industrial assembler who will consider all the parameters and the equipments capabilities to achieve the best yield in production.
3.3.1. Guide lines for package footprint adjustments

The footprint recommended in the paragraph 3.2.1 should be used to design the application motherboard. But in some cases, for industrial assembly reasons (stencil printer complexity, solder past selected, PCB material, etc…) it could be necessary to decrease the via-hole density under the package.

The impact of low via holes density below the package might have very bad effect on the device performances:

- The PCB thermal resistance will increase. Then the ambient maximum temperature must be adjusted in order to keep the case temperature (Tcase, see Figure 5) below the maximum value specified in the product datasheet.

![Figure 5: Temperature reference point (Tcase) considered in the product datasheet.](image)

Remark: A similar effect on the device thermal performances is observed when the PCB thickness increases.

- The electrical grounding of the package could be also affected. It's recommended to locate the via holes at the edges of the ground pad area and RF Pad as recommended on the UMS’s footprint drawings in order to avoid device mismatch of unsuitable propagation modes (see black filled hatched or squares on the Figure 6, the un-filled squares correspond to the thermal via holes).

![Figure 6: Example of via holes matrix on the PCB footprint.](image)
Remark: A modification of the package footprint should be done only after an analysis of the impact on the device electrical and thermal performances.

3.3.2. Guide lines for solder mask adjustments

For compact and low pitch packages as for QFN packages it’s difficult to prevent the solder bridging. Generally, a solder mask is used to avoid this kind of issues in production. The solder mask will also help to define the areas where the solder can flow and control the solder homogeneity under the package contacts (leads and exposed pad). Then the quality and the reliability of the solder join are enhanced.

The recommended solder mask clearance around the copper pads on the PCB for land pads is 70µm [2.8mils] as shown at Figure 7.

Concerning the package ground pad, it is recommended to manage an overlap of 70µm [2.8mils] minimum on the solder mask over the copper pad (see Figure 8). This configuration is suitable for self-centring of the package on the PCB footprint during reflow process.

The information’s given in this paragraph are only indicative and should not replace the design rules of the PCB manufacturer. Furthermore, the solder mask design must also take into account the final SMT assembly process used for module as well as the selected solder past characteristics.

![Figure 7: Solder mask clearance around the land pads.](image-url)
3.3.3. Recommendation for stencil printer

The choice of the stencil printer is very critical and must be done by the SMT assembler. The design of the stencil must be done in accordance with the solder paste material selected and the printing equipment capability. The guidelines given below are very general and only the assembler design rules might be considered for the product industrialization.

The solder paste deposition for a small pitch package is very sensitive to the process, and should fit with the deposition on very small surfaces like the land pads (lead contact surface is less than 0.1mm²) but also on large surfaces as for the ground pad (from 2.5mm² for a QFN 3x3 to 12mm² for a QFN 5x5).

The squeegee blade used to deposit the solder paste into the stencil cavities could bend in the larger cavities and then limit the amount of solder paste deposited. A very convenient method used to solve this issue is to split the exposed pad surface into an array more compatible with the smallest zones defined for the land pads.

In principle the stencil aperture opening above the land pad is smaller than the copper land pad (about 50µm [2 mils] in the two directions, see Figure 9).

The stencil design for the exposed pad region results from trials and evaluations on pre-serial batches in order to define the optimum pattern. Two examples of configuration are given on Figure 10.
**Figure 9**: Stencil aperture opening for land pads.

Aperture opening dimensions:
- $L - 50\mu m < Lo < L$
- $W - 50\mu m < Wo < W$

**Figure 10**: ground pad stencil examples.
4. PCB assembly

4.1. SMT assembly process flow

For the assembly process, the QFN type package can be handled as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent [2]). The use of solder is recommended, standard techniques involving solder paste and reflow process can be used (e.g. stencil solder printing, standard pick-and-place equipment, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area. The standard SMT process flow is given on the Figure 11.

![SMT process flow diagram](image)

**Figure 11 : Standard SMT process flow.**

4.2. Bill of materials

- Motherboard (typically RO4003 or equivalent, 203µm thickness).
- SMD product.
- SMD components that might be necessary.
- Solder paste (RoHS compliant, but SN63/Pb37 might be used also).
- An appropriate solder stencil printer.
- A hot plate or a reflow oven.

4.3. Component placement

UMS proposes antistatic tubes or tape&reel as standard delivery conditioning for QFN devices.

Tape&reel conditioning is appreciated for automatic SMT assembly lines. The QFN device is orientated in the tape&reel pockets as shown on Figure 12 and following the norm EIA-481 [5]. Automatic recognition systems will detect the QFN orientation in the tape&reel pocket to align the device on the PCB.

In spite of discrepancies between suppliers that could affect the recognition system (top marking aspect, the lead finish aspect), the relative position of the Pin#1 indicator on top marking to the tape&reel feeding direction is the key parameter to drive the placement process.
4.4. Reflow soldering

Five phases are necessary to solder the QFN product onto the PCB motherboard as shown on the Figure 13. The reflow temperature profile must be defined in accordance with the entire PCB module. The peak temperature when the solder melts must be defined as low as possible to avoid any damage at the device level but high enough to reach the solder melting point on the entire PCB surface despite of the thermal mass un-homogeneities.

The reflow temperature control will directly impact the mechanical robustness and the life time of the product during its operating life.

Figure 13 : Solder reflow phases.
A typical reflow profile for the UMS QFN RoHS devices (mat tin lead finish) is presented on Figure 14.

The solder thickness after reflow should be typically 50µm [2mils] and the lateral alignment between the package and the motherboard should be within 50µm [2mils].

It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or improper connections, in particular, between the ground pads on the motherboard and the package will lead to a deterioration of the RF performance and an increase of the device thermal resistance. Finally, the reliability and the lifetime of the product might be affected.
4.5. Moisture sensitivity level (MSL)

The QFN package is a non-hermetic solution, and considering that the mold compound tends to absorb moisture, some precautions have to be taken before the device assembly on PCB.

![Figure 15: Moisture absorption through the QFN mold compound.](image)

During the assembly reflow the moisture absorbed by the mold compound after storage will be vaporized. Then depending on the percentage of humidity contained in the resin, high mechanical constraints might be applied to the package.

The MSL* is an indicator for the maximum allowable time period (Floor Life Time) during which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60%RH or 85%RH before the solder reflow process:

<table>
<thead>
<tr>
<th>MSL Level</th>
<th>MSL4</th>
<th>MSL3</th>
<th>MSL2A</th>
<th>MSL2</th>
<th>MSL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floor Life</td>
<td>72hours</td>
<td>168hours</td>
<td>192hours</td>
<td>1 year</td>
<td>Unlimited</td>
</tr>
<tr>
<td>(out of bag)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>at factory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ambient</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>storage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>temperature</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
</tr>
<tr>
<td>Max.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>storage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>relative</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>humidity</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤85%RH</td>
</tr>
</tbody>
</table>

For details, refer to IPC/JEDEC J-STD-020C [2].

MLSL1 is easier to achieve on the small packages than on the large ones as QFN 4x5 and 5x5.

For MSL4 to MSL2, if during the device storage time none of the conditions below has been exceeded, the device Floor Life Time can be reset after a baking.
• Condition 1: Floor Life Time exceeded and storage conditions during this time ≤30°C and ≤60%RH.
• Condition 2: Device storage conditions have never exceeded ≤40°C and ≤85%RH.

The backing conditions are described in the table below:

<table>
<thead>
<tr>
<th>Package Body thickness ≤1.4mm</th>
<th>Bake @ 125°C</th>
<th>Bake @ 90°C ≤5%RH</th>
<th>Bake @ 40°C ≤5%RH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exceeding Floor Life by&gt;72h</td>
<td>Exceeding Floor Life by≤72h</td>
<td>Exceeding Floor Life by&gt;72h</td>
<td>Exceeding Floor Life by≤72h</td>
</tr>
<tr>
<td>Bake duration @ MSL2</td>
<td>5hours</td>
<td>3hours</td>
<td>17hours</td>
</tr>
<tr>
<td>Bake duration @ MSL2a</td>
<td>7hours</td>
<td>5hours</td>
<td>23hours</td>
</tr>
<tr>
<td>Bake duration @ MSL3</td>
<td>9hours</td>
<td>7hours</td>
<td>33hours</td>
</tr>
<tr>
<td>Bake duration @ MSL4</td>
<td>11hours</td>
<td>7hours</td>
<td>37hours</td>
</tr>
</tbody>
</table>

For details, refer to IPC/JEDEC J-STD-033B [3].

4.6. Inspection

The quality of the solder joint will be inspected by X-Ray analyse. This technique helps to detect a defective brazing quality where solder voids are present under the package exposed pad.

The solder joint quality can be also inspected on the lead edges. After the QFN singulation the lead endings of the UMS’s packages are visible at the package edges (see Figure 16). During the reflow process, the solder will melt on these surfaces. This configuration has two main advantages. Firstly, the solder joint on the lead edges help to get a robust lead to the PCB attachment. Secondly, a standard visual inspection can confirm that all the package leads are connected to the PCB.

Figure 16: QFN side view showing the lead endings after dicing.
4.7. Procedure for prototyping

The different steps are:

1. The motherboard should be cleaned with Acetone and rinsed with alcohol and DI* water. Afterwards the circuit should be fully dried.

2. The solder paste dispense should be done according to the patterns shown in the paragraph 3.3.2. It is important to note that an excessive use of solder paste can cause electrical shorts leading to poor RF performances.

3. A packaged product should be placed on the motherboard with a correct orientation and a good alignment (see the corresponding product datasheet). The alignment can be done manually by centring the packaged MMIC on the motherboard.

4. Then a reflow of the assembly should be performed on a hot plate for 5 to 6 seconds. The temperature of the plate surface should be about 240°C – 260°C.

5. The assembly should cool down completely after the reflow process.

6. The whole assembly should be finally cleaned with acetone and rinsed with alcohol and DI water.
5. Datasheet electrical information and de-embedding method for the scattering parameters exploitation

The RF performances of the QFN device might be enhanced by slight impedance re-matching on the PCB in a dedicated frequency sub-band depending on the actual specific requirements of the application. To ease such design of the custom motherboard, the Sij (scattering) parameters of the UMS device are provided in the product datasheet and can be also supplied as a Touchtone file (.s2p).

Without another notice in the product datasheet, these Sij parameters are given in the calibration plans located by de-embedding at 1.1 mm from the edge of the QFN package as shown at Figure 17.

![Figure 17: Location of the calibration plan for scattering parameters measurements.](image)
6. Annex 1: package outlines

6.1. QFN 3x3, 16 leads (QAG)

Units: mm
From the standard: JEDEC MO-220
Matt tin, lead free (Green)
6.2. QFN 3x3, 16 leads (QAG) 2RF fused Leads

Units : mm
From the standard : JEDEC MO-220
Matt tin, lead free (Green)

<table>
<thead>
<tr>
<th>1-GND</th>
<th>9-GND</th>
<th>17-GND</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-GND</td>
<td>10-RF PIN</td>
<td></td>
</tr>
<tr>
<td>3-RF PIN</td>
<td>11-GND</td>
<td></td>
</tr>
<tr>
<td>4-GND</td>
<td>12-GND</td>
<td></td>
</tr>
<tr>
<td>5-Free</td>
<td>13-Free</td>
<td></td>
</tr>
<tr>
<td>6-Free</td>
<td>14-Free</td>
<td></td>
</tr>
<tr>
<td>7-Free</td>
<td>15-Free</td>
<td></td>
</tr>
<tr>
<td>8-Free</td>
<td>16-Free</td>
<td></td>
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OUTLINE
UMS Designation: QAG Package
QFN Type: 16L QFN 3x3 Fused 2RF
Scale: 10:1
Unit: mm Projection: →
6.3. QFN 4x4, 24 leads (QDG)

Units: mm
From the standard: JEDEC MO-220
Matt tin, lead free (Green)
6.4. QFN 4x4, 24 leads (QDG) 2RF fused Leads

![Diagram of QFN 4x4 package with 2RF fused leads]

**Units:** mm

From the standard: JEDEC MO-220
Matt fin, lead free (Green)

<table>
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<tr>
<th></th>
<th>Free</th>
<th>10- Free</th>
<th>17- GND</th>
<th>25- Gnd</th>
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<td>2-</td>
<td>GND</td>
<td>10- Free</td>
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<td>4-</td>
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<td>14- GND</td>
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<td>7-</td>
<td>Free</td>
<td>15- RF PIN</td>
<td>23- Free</td>
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</tr>
<tr>
<td>8-</td>
<td>Free</td>
<td>16- GND</td>
<td>24- Free</td>
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</tr>
</tbody>
</table>

**Outline**

UMS Designation: QDG Package
QFN Type: 24L QFN 4x4 Fused 2RF
Scale: 10:1
Unit: mm
Projection: [Diagram of projection]

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6.5. QFN 4x5, 24 leads (QEG)

Units: mm
From the standard: JEDEC MO-220
Matt tin, lead free (Green)

OUTLINE
UMS Designation: QEG Package
QFN Type: 24L QFN4x5
Scale: 1:1
Unit: MM Projection: 

Subject to change without notice
6.6. QFN 5x5, 32 leads (QFG)

Units: mm
From the standard: JEDEC MO-220
Matt tin, lead free (Green)

OUTLINE
UMS Designation: QFG Package
QFN Type: 32L QFN5x5
Scale: 10:1
Unit: MM

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6.7. QFN 5x6, 36 leads (QXG)

Units: mm
From the standard: JEDEC MO-220
Matt tin, lead free (Green)

OUTLINE
UMS Designation: QXG Package
QFN Type: 36L QFN 5x6
Scale: 8:1
Unit: MM Projection:  

Subject to change without notice
6.8. QFN 6x6, 40 leads (QJG)

OUTLINE
UMS Designation: QJG Package
QFN Type: 40L QFN 6x6
Scale: 8:1
Unit: MM
Projection: 

Units : mm
From the standard : JEDEC MO-220
Matt tin, lead free (Green)
Glossary

SMD : Surface Mount Device
SMT : Surface Mount Techniques
QFN : Quad Flat Non-leaded
PCB : Printed Circuit Board
BOM : Bill Of Materials
Sij : Scattering Parameters
RoHS : Restriction of the use of certain Hazardous Substances
Lead-free : Part of the RoHS directive
DI : Deionised water
MMIC : Monolithic Microwave Integrated Circuit
THB : Temperature and Humidity Biased
HOTL : High Temperature Operating Life
Pb : Lead
MSL : Moisture Sensitivity Level
CPW : Coplanar wave guide

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