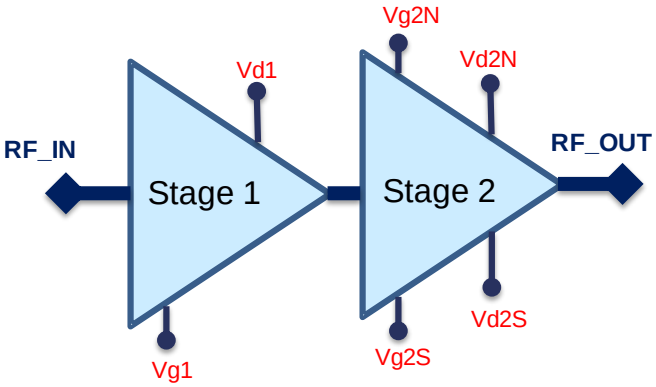
Advanced Information: AI1711

8W 5.5-7.5GHz HPA

GaN Monolithic Microwave IC



UMS has developed a packaged 8W AB class 5.5-7.5GHz High Power Amplifier. The device is a 2 stage amplifier typically exhibiting a small signal gain of 18dB with 39dBm output power at 4dB compression
The design is linearity oriented and so the device is compatible with digital baseband linearization techniques.

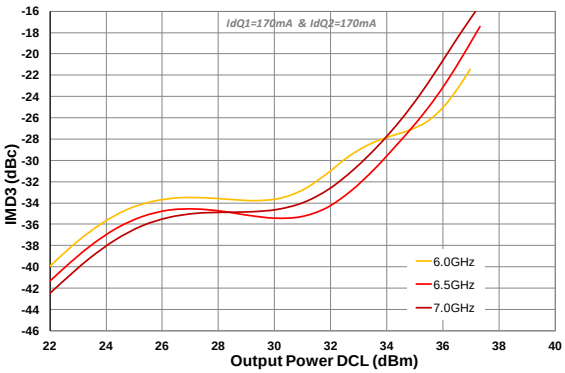
The circuit is dedicated to Point to Point telecommunication systems and is also well suited for a wide range of commercial applications.

It is developed on a robust 0.25µm gate length GaN pHEMT process. It is available in a standard surface mount 36 leads QFN6x5 package compliant with the Restriction of Hazardous Substances (RoHS) European Union directive 2011/65/EC and REACh N°1907/2006..

Main Features

- 5.5- 7.5GHz
- Psat > 39dBm
- Gain = 18dB
- C/I3 = 34dBc @10dB back-off
- MSE_{woDPD} = -27dB @30dBm
- $MSE_{withDPD}$ < -50dB @30dBm
- DC bias: Vd = 25V / IdQ = 340mA
- QFN 6x5
- MSL3

C/I3 vs Pout



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Operating Mode

Mode	Description	Pad #1, 4, 23	Pad #7, 20, 25
1	Nominal bias voltage to achieve IdQ1=170mA & IdQ2=170mA	Vg1 ≈ -3.2V Vg2N ≈ -3.4V Vg2S ≈ -3.4V	Vd1 = 25V Vd2N = 25V Vd2S = 25V

Biasing Procedure

1. Ensure Vd1=Vd2N=Vd2S=0V
2. Then bias Vgs close to Vpinch-off ➔ Vg1 = Vg2N = Vg2S ≈ -4.5V
3. Apply Vds nominal bias voltage ➔ Vd1 = Vd2N = Vd2S = 25V
4. Increase slowly Vg2N & Vg2S up to quiescent bias drain current IdQ2=170mA
5. Increase slowly Vg1 up to quiescent bias drain current IdQ1=170mA

Main Characteristics

Tamb.= +25°C, Vd = +25.0V, CW mode

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF input frequency Range	5.5		7.5	GHz
Gain	Linear Gain		18		dB
Pout	Output power at 4dB compression		39		dBm
$C/I3_{BO}$	C/I3 @30dBm		34		dBc
PAE_{max}	Power Added efficiency at 4 dB compression		30		%
PAE_{BO}	Power Added efficiency at 30dBm		10		%
|S11|	Input Return Loss (1)		8		dB
|S22|	Output Return Loss (1)		15		dB
Vg1	DC gate Voltage of stage 1		-3.2		V
Vg2	DC gate Voltage of stage 2		-3.4		V
Id	Total bias drain current at 4dB compression		1.1		A

(1) based on S-parameters measurements done on wafer (pulsed mode of gate voltage: 25µs/10%)

Recommended Maximum Ratings

Symbol	Parameter	Values	Unit
Vds	Drain bias voltage	25	V
Pdiss	Dissipated power (1)	18	W
Vg	Gate bias voltage	-5 to 0	V

(1) Considering case temperature at 80°C

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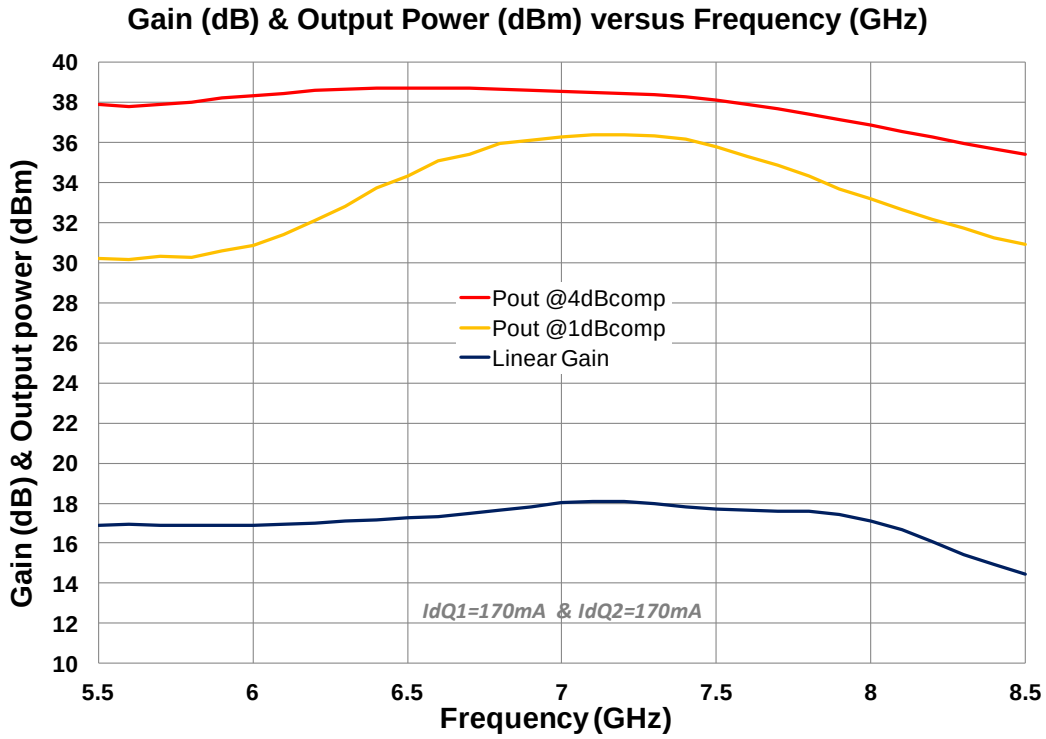
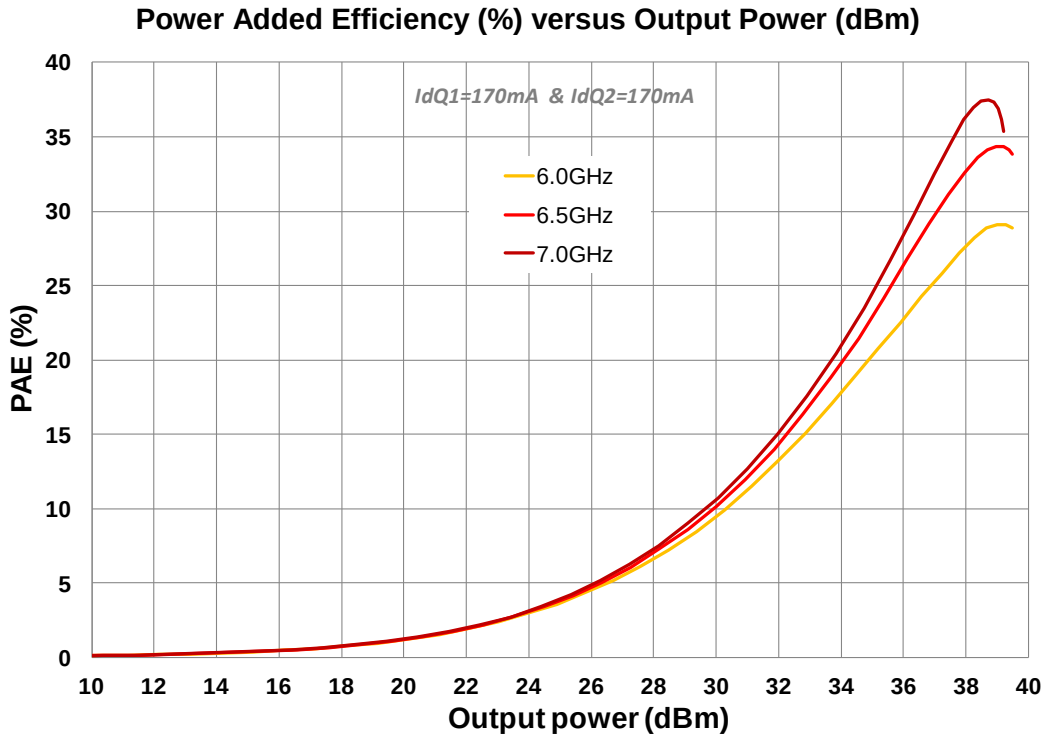
Typical in Board Measurements

Tcase=25°C, Vd=25V, IdQ1=IdQ2=170mA





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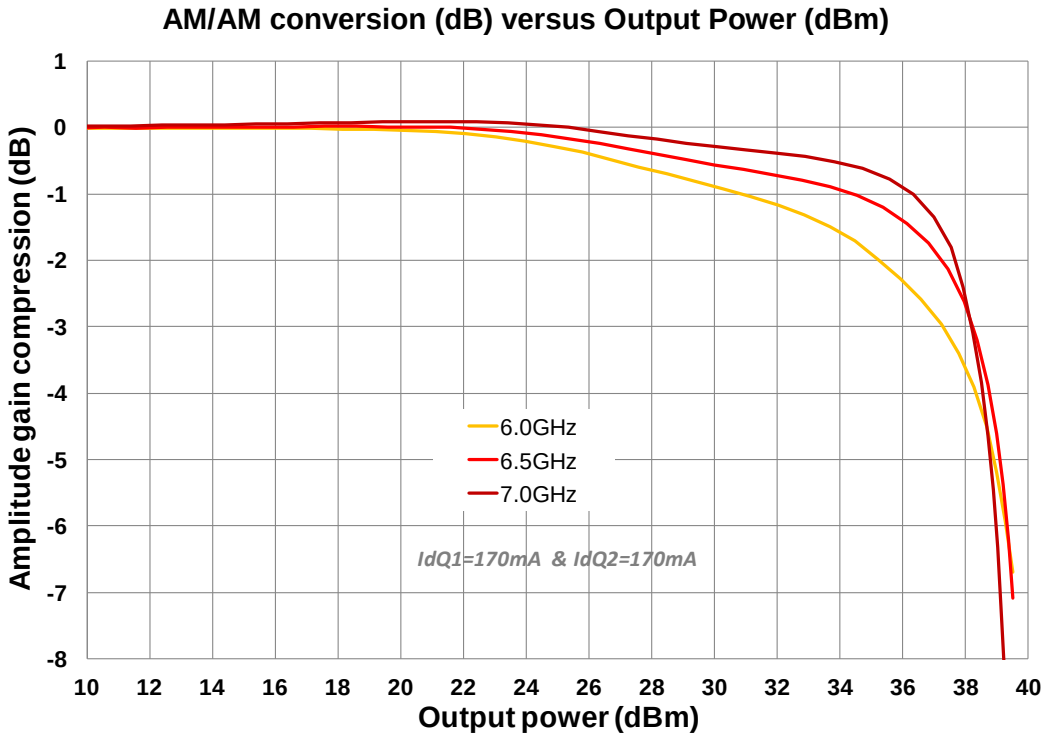
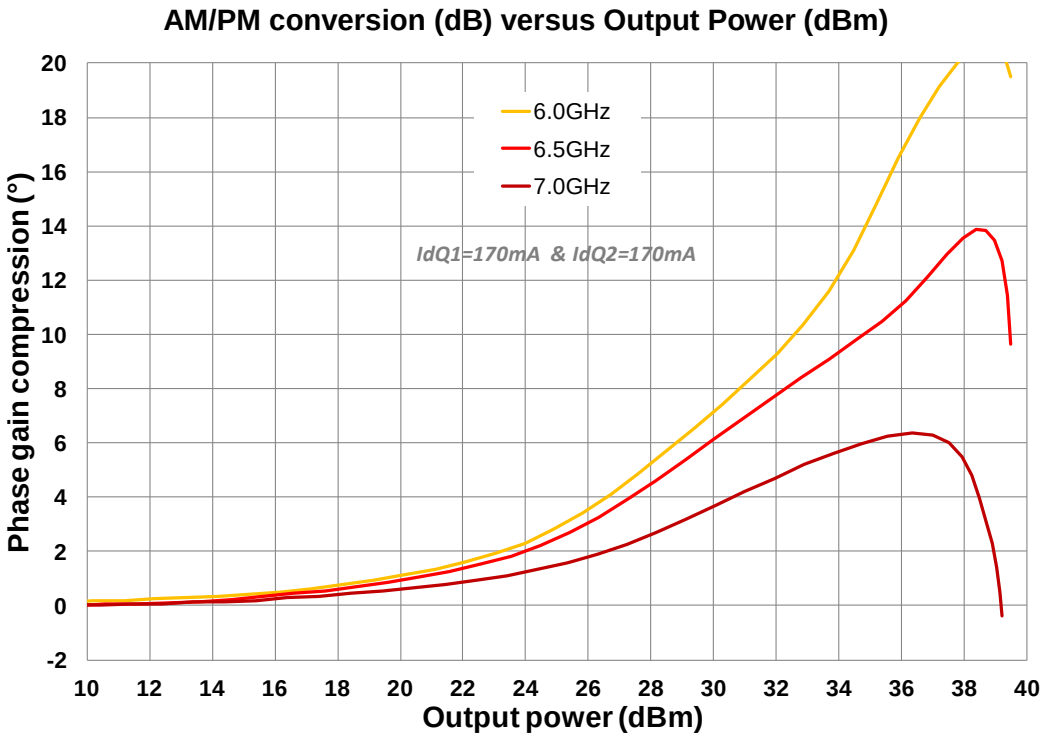
Typical in Board Measurements

Tcase=25°C, Vd=25V, IdQ1=IdQ2=170mA





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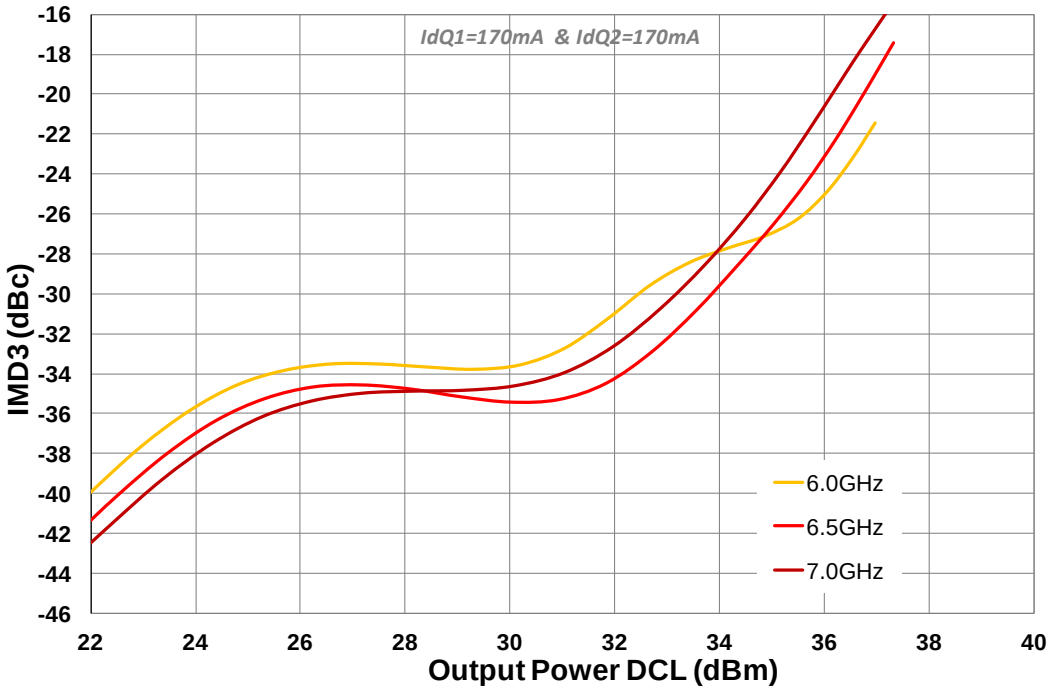
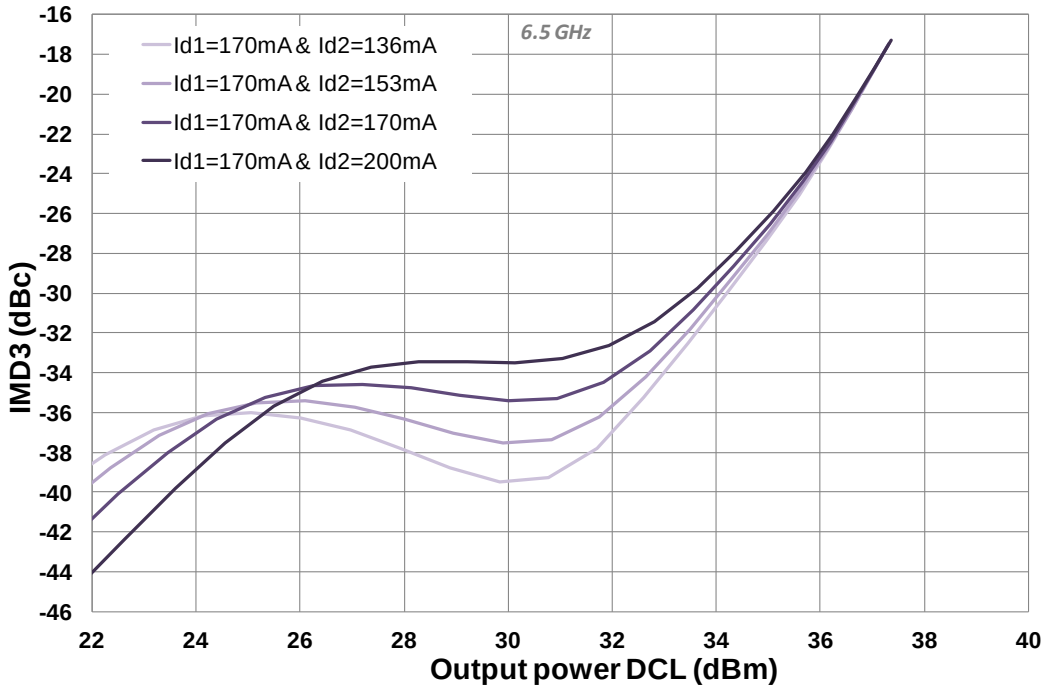
Typical in Board Measurements

Tcase=25°C, Vd=25V

IMD3 (dBc) versus Output Power (dBm) & Frequency (GHz)



IMD3 (dBc) versus Output Power (dBm) & Biasing (mA) @6.5GHz



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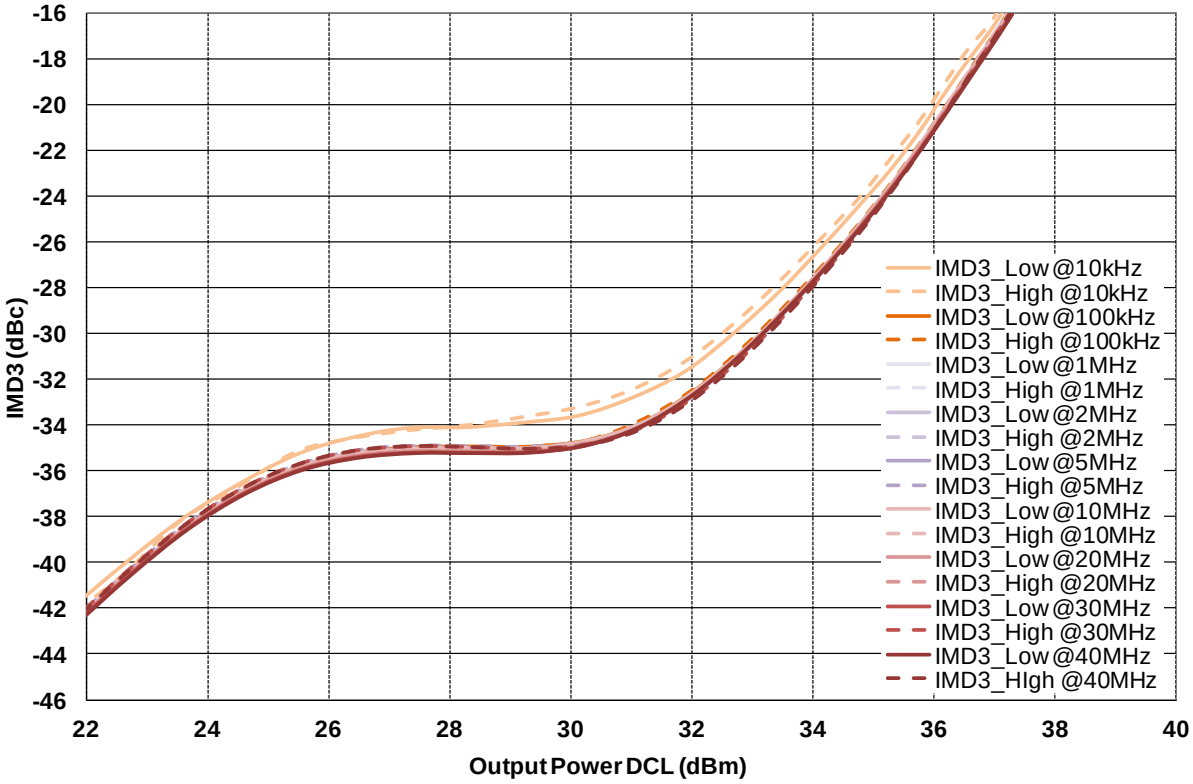
Typical in Board Measurements

Tcase=25°C, Vd=25V, IdQ1 = IdQ2 = 170 mA

IMD3 (dBc) versus Output Power (dBm) & DeltaFrequency (MHz)

Freq = 7GHz / ΔF = 10 kHz to 40MHz



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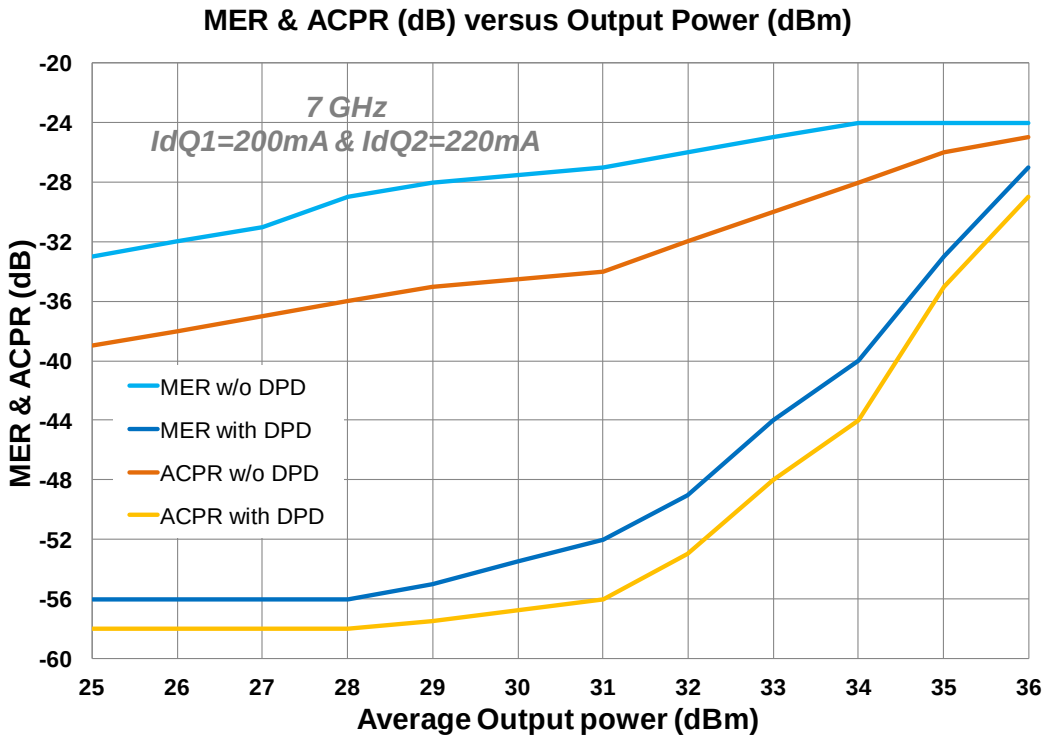
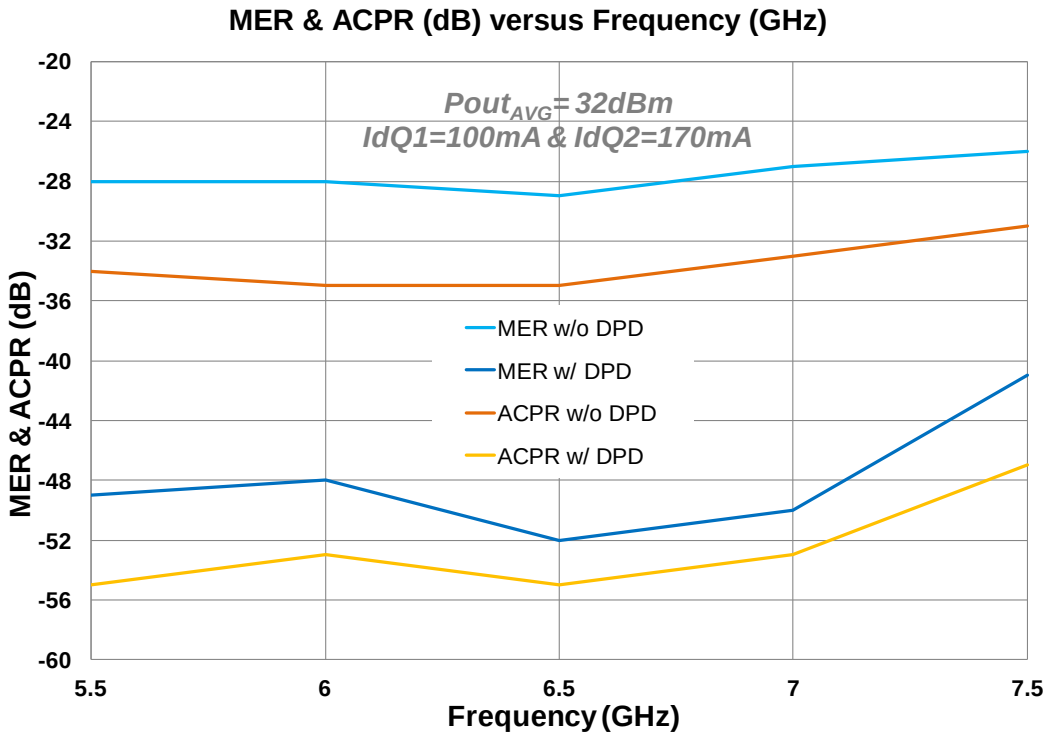
Typical in Board Measurements

Tcase=25°C, Vd=25V, QAM256 / CS=56MHz / RRC=0.2 / data random





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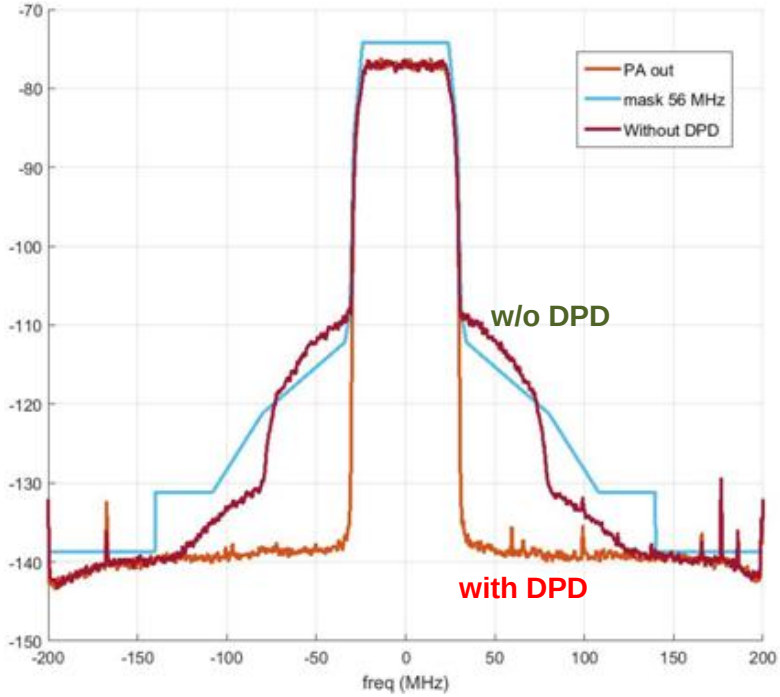
Typical in Board Measurements

Tcase=25°C, Vd=25V, QAM256 / CS=56MHz / RRC=0.2 / data random

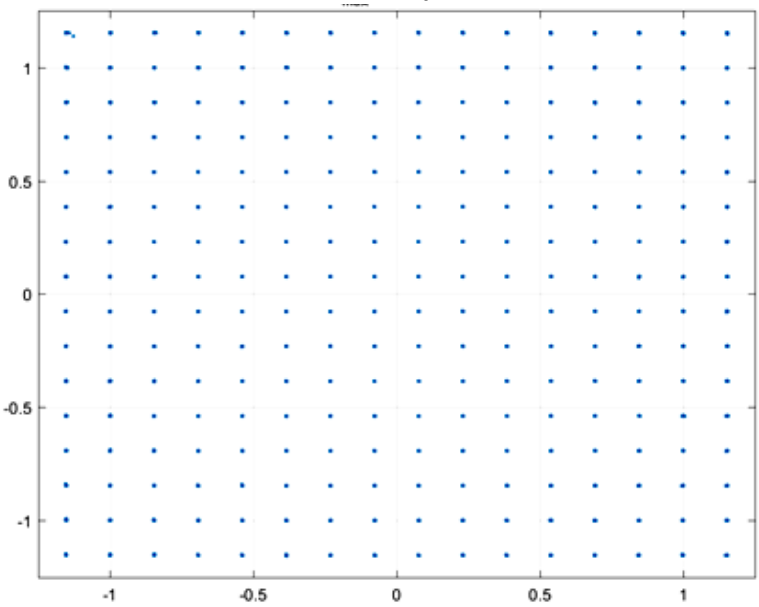
Spectrum with & w/o DPD

FRF=7GHz / $Pout_{AVG}$=30dBm / I_{DQ} = 340mA / Polynomial-DPD



Constellation with DPD

FRF=7GHz / $Pout_{AVG}$=30dBm / I_{DQ} = 340mA / Polynomial-DPD



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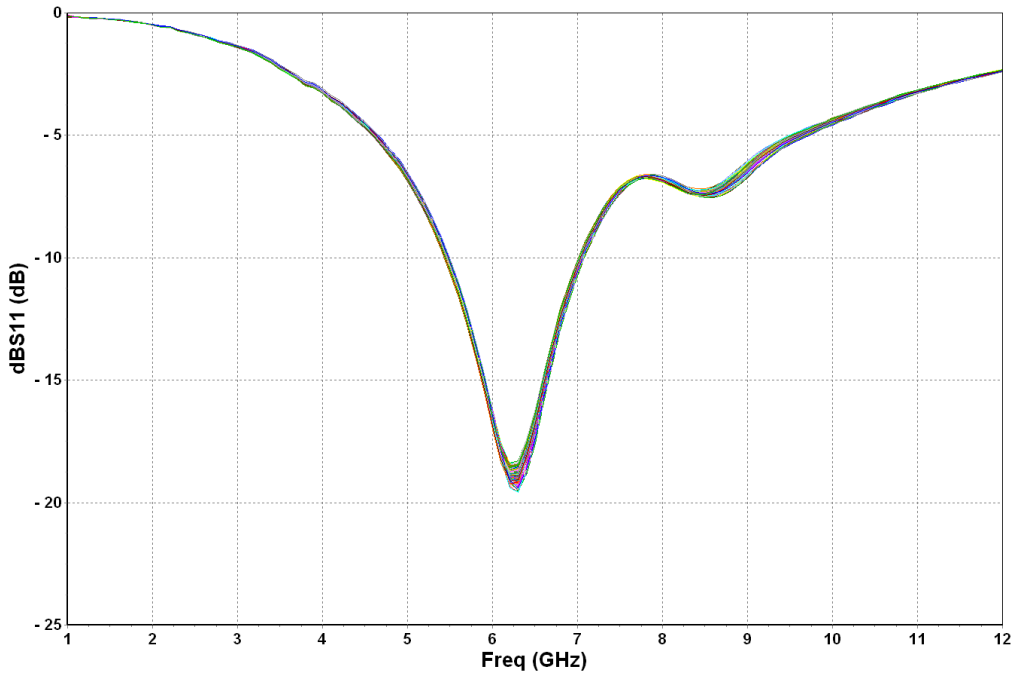
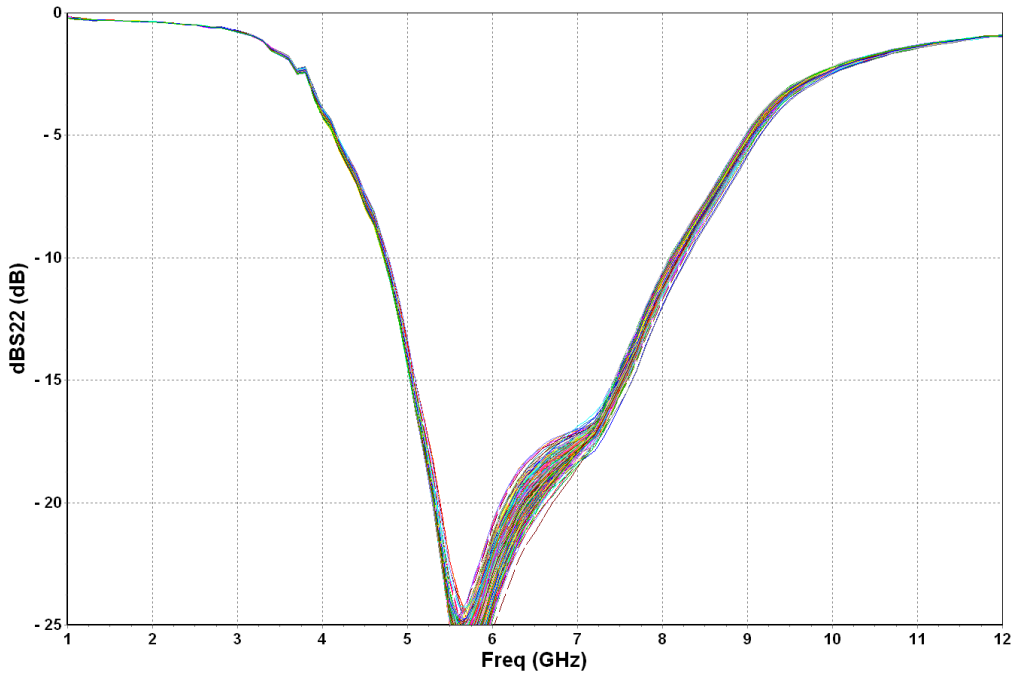
Typical On-Wafer Measurements

Conditions: Pulse Mode (25µs / 10%), Vds=25V, nominal biasing

Input return loss (dB) versus Frequency (GHz)



Output return loss (dB) versus Frequency (GHz)



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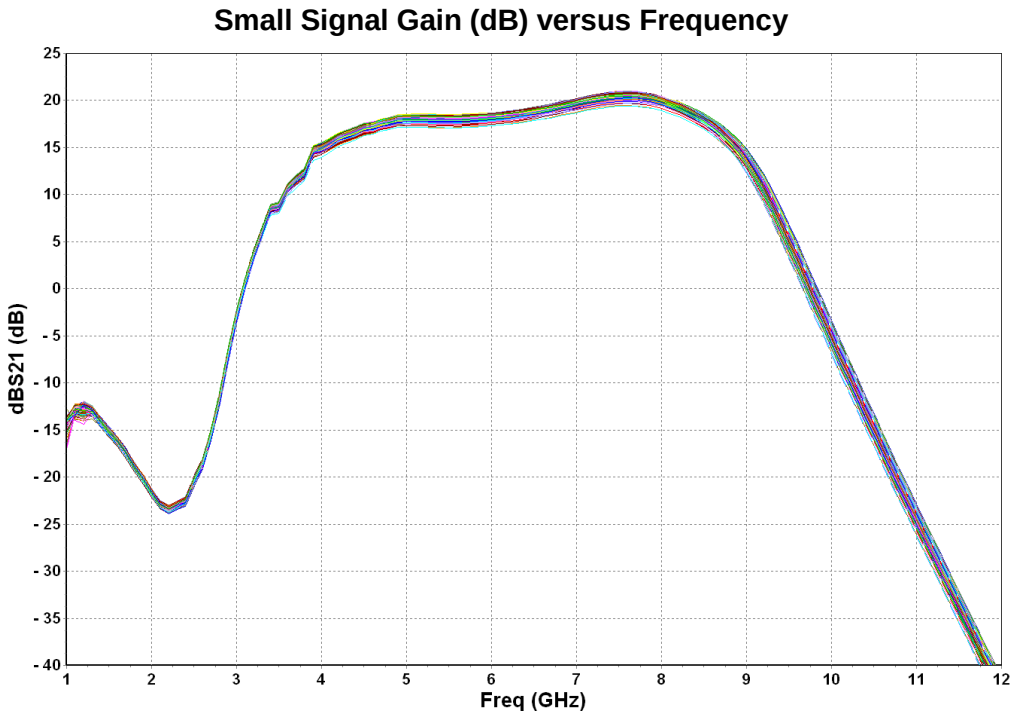

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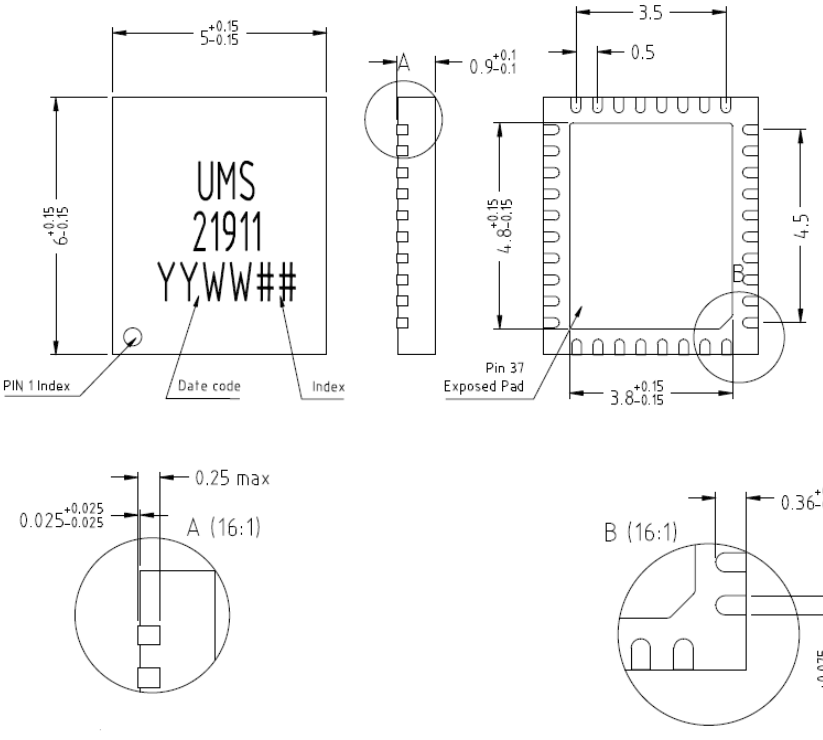
Package Outline (1)



Matte tin, Lead Free (Green)	1- Vg1	13- Gnd(2)	25- Vd1
Units : mm	2- Vg1c(3)	14- RF out	26- Gnd
From the standard : JEDEC MO-220	3- Gnd(2)	15- Gnd	27- NC
	4- Vg2S	16- NC	28- NC
37- GND	5- Vg2Sc3	17- NC	29- NC
	6- Gnd(2)	18- NC	30- Gnd(2)
	7- Vd2s	19- NC	31- RF in
	8- Gnd(2)	20- Vd2N	32- Gnd
	9- NC	21- Gnd	33- NC
	10- NC	22- Vg2Nc3	34- NC
	11- NC	23- Vg2N	35- NC
	12- NC	24- Gnd	36- NC

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

(3) It is mandatory to let the Vg1c, Vg2Nc and Vg2Sc unconnected.

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Evaluation Mother Board

■ Compatible with the proposed footprint.
■ Based on RF35P 203mm / Front side Cu 17.5mm / Back-side Cu 1 mm
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Following decoupling capacitors have been implemented on each gate and drain bias access:

- 0603 100pF ±5% 250V
- 0603 COG 1nF ±5% 100V
- 0603 X7R 10nF ±10% 100V
- 0603 X7R 100nF ±10% 100V
- 1210 X7S 10µF ±10% 50V

■ See application note AN0017 for details.
■ Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Notes

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