Application Note for Molded Plastic QFN Packages

GaAs Monolithic Packaged Microwave IC

1. General considerations on plastic molded packages

Surface Mount Device type packages (SMD*) for microwave applications are appearing more and more on the market. The use of such packages requires some specific knowledge in order to optimize the performances. In particular, the design of motherboard has a strong impact on the overall performance since the transition from the motherboard to the package is comparably large and, therefore, can lead to strong parasitic effects.

The UMS RoHS* compliant plastic QFN* packages, SMT* compatible are appreciated for their very good electrical and thermal performances at low cost. Thanks to a limited area and very short leads, they perfectly suit to the microwave circuits where the package’s parasitic elements must be as small as possible in order to be negligible at high frequency. The best trade-off between electrical performances and industrial constraints is get with a lead to lead pitch of 0.5mm. Today, excellent performances are demonstrated up-to 40GHz. And the performances of the packaged products are similar to the equivalent bare-dies when the package model is taken into account in MMIC* design.

The lead-frame structure made of copper (C194 alloy) includes small leads but also a large metallic exposed-pad acting as an efficient ground-pad and a thermal drain to the PCB* circuit. So, the thermal and electrical ground paths are optimum, and the embedded MMIC is working in very good conditions (see Figure 1).

Figure 1 : QFN package outline.

* See Glossary
The packages are LASER marked on top-side as shown on the Figure 1. The package top marking includes a Pin#1 index and three lines of text used for the device identification.

- Line 1: UMS logo.
- Line 2: device part number.
- Line 3: date code
  - YY stands for the two last digits of the assembly year.
  - WW stands for the week in the assembly year (from 01 to 52).
  - ZZ are two optional characters used internally at UMS for lot identification.

**Remark:** In some cases, samples or prototypes can be marked with white ink.

The mold protection of the plastic QFN acts as a very good mechanical protection for SMT handling steps. When required, the QFN product qualification includes a THB* 85°C / 85% RH / 1000 hours test and a HTOL* / 1000 hours test [4].

The UMS’s QFN plastic packages are compliant with RoHS directive (Pb* free). The list of the materials constituting the product is given on the Figure 2.

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Material</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MMIC</td>
<td>GaAs</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Die attach</td>
<td>Epoxy resin with silver filler</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Bonding Wire</td>
<td>Gold</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Frame</td>
<td>Copper (C194) with Sn external finish</td>
<td>Sn finish on back side, see 4a</td>
</tr>
<tr>
<td>4a</td>
<td>Frame external Sn  finish</td>
<td>Matte tin (Sn), thickness 400 μinch</td>
<td>Package's exposed surfaces only</td>
</tr>
<tr>
<td>5</td>
<td>Lead</td>
<td>Copper (C194) with Sn external finish</td>
<td>Sn finish on top side, see 5b</td>
</tr>
<tr>
<td>5a</td>
<td>Lead external Sn  finish</td>
<td>Matte tin (Sn), thickness 400 μinch</td>
<td>Package's exposed surfaces only</td>
</tr>
<tr>
<td>5b</td>
<td>Lead bond pad Ag finish</td>
<td>Silver spots (Ag), thickness &lt;40 μinch</td>
<td>Lead's internal bond area</td>
</tr>
<tr>
<td>6</td>
<td>Mold Resin</td>
<td>Multi-Aromatic Resin (Br/St free)</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2:** QFN products build-up structure.
The QFN devices are designed to be mounted onto any standard PCB compatible with SMT process. But, of course at millimetre-wave frequencies a special care must be taken at the PCB level to manage a good electrical and thermal matching of the device. This application note gives guide lines and recommendations in order to design the appropriate motherboard and take advantage of the best circuit performances.

2. UMS’s QFN packages outlines

Considering the specificities of the microwave products and the impact of the package on the device performances, UMS proposes four types of over-molded plastic package. This family of packages perfectly answers to the high performances objectives and takes advantage of the standard low cost solutions available today for mass production.

<table>
<thead>
<tr>
<th>Package case</th>
<th>UMS designation</th>
<th>Package Outlines</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 3x3, 16 leads</td>
<td>QAG</td>
<td>See annex 6.1</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads</td>
<td>QDG</td>
<td>See annex 6.2</td>
</tr>
<tr>
<td>QFN 4x5, 24 leads</td>
<td>QEG</td>
<td>See annex 6.3</td>
</tr>
<tr>
<td>QFN 5x5, 28 leads</td>
<td>QGG</td>
<td>See annex 6.4</td>
</tr>
</tbody>
</table>

The package outlines have been defined based on the JEDEC MO-220 standard [1]. The tolerances indicated on the drawings have been calculated to comply with the standard of several suppliers in order to propose the best industrial solution regarding the application needs like production volumes, cost, etc…

Please download periodically from the UMS web site (http://www.ums-gaas.com) the latest version of this application note to be certain to get the latest version of the drawings.

3. PCB design

3.1. General considerations for PCB design

The products developed by UMS are tested on an evaluation board in order to guarantee the best performances at the customer level in the final equipment. Since the internal design of the GaAs MMIC is generally based on a micro-strip structure, the motherboard where the QFN device will be mounted should be designed in accordance with this configuration. The motherboard acts as a:

**Signal feeding structure to the QFN device:** Transmission lines are needed on the PCB. For electromagnetic reasons, a micro-strip mode is generally chosen and helps to avoid parasitic propagations modes on the PCB. It will also help to minimize the electrical transmission losses. The UMS’ QFN packages are generally designed to be matched on 50Ω loads. However, the motherboard in the close area around the QFN device should be designed to have a good impedance transition from the micro-strip
line to the package leads. The device foot-prints proposed in the paragraph “UMS PCB” are optimized to manage this transition.

**QFN device electrical grounding to the sub-system ground:** Since the QFN device at millimetre-wave frequencies contains generally a GaAs micro-strip chip, it is necessary to provide a very good grounding of the package to the PCB’s ground. The main ground interface between the package and the motherboard is done through the package exposed pad (see Figure 1) which is soldered to the PCB’s ground pad (see Figure 3) in the case of a SMT mounting process. The link between the ground of the sub-system and the ground pad on the motherboard is generally done using a metallic via-hole structure. A very standard configuration with metallic via holes to connect the sub-system ground at the PCB’s back-side interface to the package exposed pad is presented Figure 4.

**QFN device thermal connection to the sub-system heat-sink:** The QFN package thanks to its copper lead-frame has very good thermal performances. The dissipated power is easily spread out from the package through the exposed pad to the PCB. The via holes in the PCB will act as thermal drain to dissipated to thermal energy to the heat-sink of the sub-system (see Figure 4).

![Figure 3: General overview of a QFN motherboard.](image)

![Figure 4: Cross section view of a QFN device assembled on a micro-strip carrier (PCB).](image)
3.2. UMS PCBs for prototyping

SMD type packages from UMS allow design and fabrication of mm-wave modules at low cost. Therefore, a suitable motherboard environment was chosen according to this aim. All tests and verifications were performed on Rogers RO4003. This material has a permittivity of 3.38 and is used with a thickness of 203µm [8mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line should have a strip width of about 460µm [approximately 18mils]. Other materials with similar properties can be used as well.

The evaluation motherboards proposed in this application note were designed for prototyping and manual assembly. They lead to get the best product performances after assembly.

The product datasheet generally includes the recommended motherboard used for the product characterization. Sometimes, slight differences can be observed between the motherboard proposed in the datasheet and the typical motherboard recommended in this application note. These differences might come from product specificities, but generally the land-pattern is strictly equivalent to those proposed in the next paragraph.

It is recommended to use as much as possible the proposed layout and technology shown in the product’s datasheet in order to achieve the best performances out of the packaged product.

3.2.1. Recommended package land-pattern and package foot-print

The contact areas on the motherboard for the package connections should be designed according to the foot-prints given in the following table:

<table>
<thead>
<tr>
<th>Package case</th>
<th>UMS designation</th>
<th>Package foot-print drawings</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 3x3, 16 leads</td>
<td>QAG</td>
<td>See annex 6.5</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads</td>
<td>QDG</td>
<td>See annex 6.6</td>
</tr>
<tr>
<td>QFN 4x5, 24 leads</td>
<td>QEG</td>
<td>See annex 6.7</td>
</tr>
<tr>
<td>QFN 5x5, 28 leads</td>
<td>QGG</td>
<td>See annex 6.8</td>
</tr>
</tbody>
</table>

The foot-print layout for the motherboard as given in the product datasheet is adapted to get the best performance out of the product and, therefore, can differ from product to product.

A proper via structure under the ground pad is very important in order to achieve a good RF and thermal performances. All tests have been done by using a grid of plated via holes through the substrate with a diameter of less than 300µm [12mils] and a spacing lower than 700µm [28mils] from the centres of two adjacent via holes. Via holes grid should cover the whole area of the ground pad. The nearest via holes to the RF ports should be as close as possible of the ground pad edges to allow a good RF ground connection. Since via holes are also important for heat transfer, a
proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between the package and the heat sink. However, it is important to consider that via holes internal copper plating will always act as the main thermal drain.

Via filling is also recommended for SMT assembly reasons. Conductive epoxy or any other appropriate thermal conductive material can be used before solder past deposition in order to avoid solder wicking into via holes during the reflow process. This configuration will help to decrease the thermal resistance of the PCB structure, but it will also avoid low package stand-off height.

For the power devices the use of heat slugs in the motherboard instead of a grid of via’s is recommended.

The table hereafter gives the via holes geometry for each package type.

<table>
<thead>
<tr>
<th>Via-hole external diameter (mm)</th>
<th>QFN 16L 3x3</th>
<th>QFN 24L 4x4</th>
<th>QFN 24L 4x5 (or 5x4)</th>
<th>QFN 28L 5X5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via-hole internal diameter (mm)</td>
<td>0.30</td>
<td>0.30</td>
<td>0.30</td>
<td>0.30</td>
</tr>
<tr>
<td>Number of vias under the package</td>
<td>4</td>
<td>12</td>
<td>24</td>
<td>36</td>
</tr>
<tr>
<td>Via holes pitch (mm)</td>
<td>0.70</td>
<td>0.70</td>
<td>0.60</td>
<td>0.60</td>
</tr>
<tr>
<td>Via holes height (=PCB thickness) (mm)</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
<td>0.203</td>
</tr>
<tr>
<td>$R_{th,PCB,UMS}$: Estimated thermal resistance equivalent to the package foot-print on PCB (°C/W)</td>
<td>5.7</td>
<td>1.9</td>
<td>1.0</td>
<td>0.6</td>
</tr>
</tbody>
</table>

### 3.2.2. UMS’s motherboards layouts

Besides of the package foot-prints described above, the evaluation motherboards includes transmission lines for the microwave signals and DC path to bias the component. Thanks to advanced design techniques, the MMICs which are designed to be embedded in plastic packages have a very good intrinsic stability. So no decoupling capacitor is needed in the QFN package. The decoupling circuits can be reported directly on the PCB using high quality SMD components as close as possible from the QFN package. This configuration helps to get the lower cost solution at the sub-system level.

Generic evaluation motherboards are given for each package in the following table:

<table>
<thead>
<tr>
<th>Package case</th>
<th>UMS designation</th>
<th>Motherboard drawings</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 3x3, 16 leads</td>
<td>QAG</td>
<td>See annex 6.9</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads</td>
<td>QDG</td>
<td>See annex 6.10</td>
</tr>
<tr>
<td>QFN 4x5, 24 leads</td>
<td>QEG</td>
<td>See annex 6.11</td>
</tr>
<tr>
<td>QFN 5x5, 28 leads</td>
<td>QGG</td>
<td>See annex 6.12</td>
</tr>
</tbody>
</table>
3.3. Motherboard design for large production volumes (SMT process)

The application’s motherboard should be designed to be as close as possible to the UMS’s PCB recommended in the datasheet, and then also complying with the constraints of the industrial SMT processes. Large volumes production equipments and fully automatic SMT assembly lines have specific requirements to be taken into account for the application’s PCB design. A large set of parameters will influence the industrial assembly process and the final assembly yield like:

- the PCB stack-up structure
- the PCB materials properties
- the PCB thermal capacitance
- the solder paste properties
- the fabrication tolerances of the stencil printer
- the placement tool agility and repeatability
- the solder paste reflow profile and the oven properties

Since it is not possible to give generic motherboard layout fully compatible with all the industrial SMT processes in this document, this paragraph intent only to give some guidelines, but it should not replace the design rules provided by the industrial assembler who will consider all the parameters and the equipments capabilities to achieve the best yield in production.

3.3.1. Package foot-print adjustments for automatic SMT assembly process

The foot-print recommended in the paragraph 3.2.1 must be used to design the application motherboard. But in some cases, for industrial assembly reasons (stencil printer complexity, solder past selected, PCB material, etc…) it could be necessary to decrease the via-hole density under the package.

The impact of low via holes density below the package might have very bad effect on the device performances:

- The PCB thermal resistance will increase. Then the ambient maximum temperature must be adjusted in order to keep the case temperature (Tcase, see Figure 5) below the maximum value specified in the product datasheet.

![Figure 5: Temperature reference point (Tcase) considered in the product datasheet.](image)
Remark: A similar effect on the device thermal performances is observed when the PCB thickness increases.

- The electrical grounding of the package could be also affected. It’s recommended to locate the via holes at the edges of the ground pad area as recommended on the UMS’s foot-print drawings in order to avoid device mismatch of unsuitable propagation modes (see filled scares on the Figure 6, the un-filled scares correspond to thermal via holes).

![Figure 6: Via holes location (package foot-print QFN 16L 4x4).](image)

Remark: A modification of the package foot-print should be done only after an analysis of the impact on the device electrical and thermal performances.

### 3.3.2. Solder mask design recommendations

For compact and low pitch packages as for QFN packages it is difficult to prevent the solder bridging. Generally, a solder mask is used to avoid this kind of issues in production. The solder mask will also help to define the areas where the solder can flow and control the solder homogeneity under the package contacts (leads and exposed pad). Then the quality and the reliability of the solder join are enhanced.

The recommended solder mask clearance around the copper pads on the PCB for land pads is 70µm [2.8mils] as shown on the Figure 7. Concerning the package ground pad, it is recommended to manage an overlap of 70µm [2.8mils] minimum on the solder mask over the copper pad (see Figure 8). This configuration is suitable for self-centring of the package on the PCB foot-print during reflow process.

Remark: The information’s given in this paragraph are only indicative and should not replace the design rules of the PCB manufacturer. Furthermore, the solder mask design must also take into account the final SMT assembly process used for module as well as the selected solder past characteristics.
3.3.3. Stencil printer recommendations

The choice of the stencil printer is very critical and must be done by the SMT assembler. The design of the stencil must be done in accordance with the solder paste material selected and the printing equipment capability. The guidelines given in the table below should be followed:

<table>
<thead>
<tr>
<th>Package case</th>
<th>UMS designation</th>
<th>Package foot-print drawings</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 3x3, 16 leads</td>
<td>QAG</td>
<td>See annex 6.5</td>
</tr>
<tr>
<td>QFN 4x4, 24 leads</td>
<td>QDG</td>
<td>See annex 6.6</td>
</tr>
<tr>
<td>QFN 4x5, 24 leads</td>
<td>QEG</td>
<td>See annex 6.7</td>
</tr>
<tr>
<td>QFN 5x5, 28 leads</td>
<td>QGG</td>
<td>See annex 6.8</td>
</tr>
</tbody>
</table>
below are very generic and only the assembler design rules might be considered for the product industrialization.

The solder paste deposition for a small pitch package is very sensitive to the process, and should fit with the deposition on very small surfaces like the land pads (lead contact surface is less than 0.1mm²) but also on large surfaces as for the ground pad (from 2.5mm² for a QFN 3x3 to 12mm² for a QFN 5x5).

The squeegeee blade used to deposit the solder paste into the stencil cavities could bend in the larger cavities and then limit the amount of solder paste deposited. A very convenient method used to solve this issue is to split the exposed pad surface into an array more compatible with the smallest zones defined for the land pads.

Generally the stencil aperture opening above the land pad is smaller than the copper land pad (about 50µm [2 mils] in the two directions, see Figure 9).

The stencil design for the exposed pad region results from trials and evaluations on pre-serial batches in order to define the optimum pattern. Two examples of configuration are given on Figure 10.

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**Figure 9 : Stencil aperture opening for land pads.**

**Figure 10 : ground pad stencil examples.**

Aperture opening dimensions:

- \( L - 50\mu m < L_0 < L \)
- \( W - 50\mu m < W_0 < W \)
4. PCB assembly

4.1. SMT assembly process flow

For the assembly process, the QFN type package can be handled as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent [2]). The use of solder is recommended, standard techniques involving solder paste and reflow process can be used (e.g. stencil solder printing, standard pick-and-place equipment, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area. The standard SMT process flow is given on the Figure 11.

![Figure 11: Standard SMT process flow.](image)

4.2. Bill of materials

- Motherboard (typically RO4003 or equivalent, 203µm thickness).
- SMD product.
- SMD components that might be necessary.
- Solder paste (RoHS compliant, but SN63/Pb37 might be used also).
- An appropriate solder stencil printer.
- A hot plate or a reflow oven.

4.3. Component placement

UMS proposes antistatic tubes or tape&reel as standard delivery conditioning for QFN devices. Tape&reel conditioning is appreciated for automatic SMT assembly lines. The QFN device is orientated in the tape&reel pockets as shown on Figure 12 and following the norm EIA-481 [5]. Automatic recognition systems will detect the QFN orientation in the tape&reel pocket to align the device on the PCB. In spite of discrepancies between suppliers that could affect the recognition system (top marking aspect, the lead finish aspect), the relative position of the Pin#1 indicator on top marking to the tape&reel feeding direction is the key parameter to drive the placement process.
4.4. Reflow soldering

Five phases are necessary to solder the QFN product onto the PCB motherboard as shown on the Figure 13. The reflow temperature profile must be defined in accordance with the entire PCB module. The peak temperature when the solder melts must be defined as low as possible to avoid any damage at the device level but high enough to reach the solder melting point on the entire PCB surface despite of the thermal mass un-homogeneities. The reflow temperature control will directly impact the mechanical robustness and the life time of the product during its operating life.

A typical reflow profile for the UMS QFN RoHS devices (mat tin lead finish) is presented on Figure 14.
MAXIMUM RECOMMENDED REFLOW PROFILE for LEADFREE SMT ASSEMBLY PRODUCTS

Figure 14: Recommended reflow temperature profile for lead free solder (RoHS).

The solder thickness after reflow should be typically 50µm [2mils] and the lateral alignment between the package and the motherboard should be within 50µm [2mils].

It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or improper connections, in particular, between the ground pads on the motherboard and the package will lead to a deterioration of the RF performance and an increase of the device thermal resistance. Finally, the reliability and the lifetime of the product might be affected.

4.5. Moisture sensitivity level (MSL)

The QFN package is a non-hermetic solution, and considering that the mold compound trends to absorb moisture, some precautions have to be taken before the device assembly on PCB.

Figure 15: Moisture absorption through the QFN mold compound.
During the assembly reflow the moisture absorbed by the mold compound after storage will be vaporized. Then depending on the percentage of humidity contained in the resin, high mechanical constraints might be applied to the package.

The MSL* is an indicator for the maximum allowable time period (Floor Life Time) during which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60%RH or 85%RH before the solder reflow process:

<table>
<thead>
<tr>
<th>MSL Level</th>
<th>MSL4</th>
<th>MSL3</th>
<th>MSL2A</th>
<th>MSL2</th>
<th>MSL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floor Life (out of bag) at factory ambient</td>
<td>72hours</td>
<td>168hours</td>
<td>192hours</td>
<td>1year</td>
<td>Unlimited</td>
</tr>
<tr>
<td>Max. storage temperature</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
<td>≤30°C</td>
</tr>
<tr>
<td>Max. storage relative humidity</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤60%RH</td>
<td>≤85%RH</td>
</tr>
</tbody>
</table>

For details, refer to IPC/JEDEC J-STD-020C [2].

UMS standard offer is from MSL2 to MSL1. MLS1 is easier to achieve on the small packages than on the large ones as QFN 4x5 and 5x5.

For MSL4 to MSL2, if during the device storage time none of the conditions below has been exceeded, the device Floor Life Time can be reset after a baking.

- Condition 1: Floor Life Time exceeded and storage conditions during this time ≤30°C and ≤60%RH.
- Condition 2: Device storage conditions have never exceeded ≤40°C and ≤85%RH.

The backing conditions are described in the table below:

<table>
<thead>
<tr>
<th>Package Body thickness ≤1.4mm</th>
<th>Bake @ 125°C</th>
<th>Bake @ 90°C ≤5%RH</th>
<th>Bake @ 40°C ≤5%RH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exceeding Floor Life by&gt;72h</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bake duration @ MSL2</td>
<td>5hours</td>
<td>17hours</td>
<td>8days</td>
</tr>
<tr>
<td>Bake duration @ MSL2a</td>
<td>7hours</td>
<td>23hours</td>
<td>9days</td>
</tr>
<tr>
<td>Bake duration @ MSL3</td>
<td>9hours</td>
<td>33hours</td>
<td>13days</td>
</tr>
<tr>
<td>Bake duration @ MSL4</td>
<td>11hours</td>
<td>37hours</td>
<td>15days</td>
</tr>
</tbody>
</table>

For details, refer to IPC/JEDEC J-STD-033B [3].
4.6. Inspection

The quality of the solder joint will be inspected by X-Ray analyse. This technique helps to detect a defective brazing quality where solder voids are present under the package exposed pad.

The solder joint quality can be also inspected on the lead edges. After the QFN singulation the lead endings of the UMS’s packages are visible at the package edges (see Figure 16). During the reflow process, the solder will melt on these surfaces. This configuration has two main advantages. Firstly, the solder joint on the lead edges help to get a robust lead to the PCB attachment. Secondly, a standard visual inspection can confirm that all the package leads are connected to the PCB.

![Figure 16: QFN side view showing the lead endings after dicing.](image)

4.7. Procedure for prototyping

The different steps are:

1. The motherboard should be cleaned with Acetone and rinsed with alcohol and DI* water. Afterwards the circuit should be fully dried.

2. The solder paste dispense should be done according to the patterns shown in the paragraph 3.3.2. It is important to note that an excessive use of solder paste can cause electrical shorts leading to poor RF performances.

3. A packaged product should be placed on the motherboard with a correct orientation and a good alignment (see the corresponding product datasheet). The alignment can be done manually by centring the packaged MMIC on the motherboard.

4. Then a reflow of the assembly should be performed on a hot plate for 5 to 6 seconds. The temperature of the plate surface should be about 240°C – 260°C.

5. The assembly should cool down completely after the reflow process.

6. The whole assembly should be finally cleaned with acetone and rinsed with alcohol and DI water.
5. Datasheet electrical information and de-embedding method for the scattering parameters exploitation

The RF performances of the QFN device might be enhanced by external (on motherboard) specific shapes for the input and output RF lines, providing local re-matching (using stub and/or slug) in a dedicated frequency sub-band. To ease the design of the custom motherboard layout, the $S_{ij}$ (scattering) parameters are provided in the product datasheet. These $S_{ij}$ parameters are measured on the motherboard recommended in the product datasheet. The corresponding Touchtone compatible files (.s2p) can be also downloaded from the UMS’s web site.

In order to design the appropriate matching network on the PCB, it is necessary to take into account the location of the calibration plans used for the scattering parameters measurement included to the product data-sheet (Figure 17). These drawings show the distance in millimetres from the centre of the QFN device to the access ports where the $S_{ij}$ parameters are given for each of the QFN's used by UMS.

![Figure 17: Calibration plans for $S_{ij}$ measurements reported in the product datasheet (drawings not to scale).](image)

<table>
<thead>
<tr>
<th>QFN 16L 3x3</th>
<th>QFN 24L 4x4 (or 4x5)</th>
<th>QFN 28L 5x5 (or 5x4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{ij}$ access ports to package centre distance</td>
<td>2.65 mm</td>
<td>3.18 mm</td>
</tr>
</tbody>
</table>

Ports to package-centre distance considered for the $S_{ij}$ measurements reported in the product datasheet.
6. Annexes

6.1. QFN 3x3, 16 leads outline

Units: mm
From the standard: JEDEC MO-220 [VEED]
Matt tin, Lead free (Green)
6.2. QFN 4x4, 24 leads outline

Units: mm
From the standard: JEDEC MO-220 [VGGD]
Matt tin, Lead free (Green)
6.3. QFN 4x5, 24 leads outline

From the standard: JEDEC MO-220 [VGH01]
Matt tin, Lead free (Green)

Units: mm
6.4. QFN 5x5, 28 leads outline

Units: mm
From the standard: JEDEC MO-220 (VHHD)
Matt Tin, Lead-free (Green)
6.5. Recommended foot-print for QFN 3x3, 16 leads

**RECOMMENDED FOOTPRINT FOR 16L QFN3X3**

**RECOMMENDED SOLDER MASK FOR 16L QFN3X3**

**Material**: Ro4003 ROGERS

- **ε**: 3.38
- **Thickness**: 203µm (0.008"

This Footprint is used for UMS prototyping assembly. For production, design must be adapted with regard to PCB tolerances and assembly process.

The location of the RF lines is indicative and must be adjusted device by device but the same type of land pattern must be used.

DXF file available on UMS website
http://www.ums-gaas.com

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**FOOTPRINT**

- **Part number**: 61 495 473
- **Type**: 043
- **Designation**: Recommended Footprint 16L QFN3X3
- **Scale**: 10:1
- **Name**: Belloche
- **Rev.**: C
- **Format**: A
- **Sheet**: 01 of 01
- **Date**: 06/04/04

---

Ref. AN0017-8206 - 26 Jun 08  21/32 Subject to change without notice
6.6. Recommended foot-print for QFN 4x4, 24 leads

Material: Ro4003 ROGERS
\( \varepsilon_r = 3.38 \)
Thickness: 203\( \mu \)m (0.008")

This footprint is used for UMS prototyping assembly. For production, design must be adapted with regard to PCB tolerances and assembly process.

The location of the RF lines is indicative and must be adjusted device by device but the same type of land pattern must be used.

DXF file available on UMS web site
http://www.ums-gaas.com

C Add solder mask
B Ground footprint optimization – Via holes pitch modification
A Add ground foot-print – Add microstrip line – Add material – Add QFN pins

Ref. : AN0017-8206 - 26 Jun 08 22/32 Subject to change without notice

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - BP46 - 91401 Orsay Cedex France
Tel.: +33 (0)1 69 33 03 08 - Fax: +33 (0)1 69 33 03 09
6.7. Recommended foot-print for QFN 4x5, 24 leads

Material: Ro4003 ROGERS
E = 3.38
Thickness= 203μm (0.008")

This footprint is used for UMS prototyping assembly. For production, design must be adapted with regard to PCB tolerances and assembly process.

The location of the RF lines is indicative and must be adjusted device by device but the same type of land pattern must be used.

DXF file available on UMS web site
http://www.ums-gsas.com

**FOOTPRINT**

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Ref.: AN0017-8206 - 26 Jun 08 23/32 Subject to change without notice
6.8. Recommended foot-print for QFN 5x5, 28 leads

Material: Ro4003 ROGERS
ε = 3.38
Thickness= 203µm (0.008")

This footprint is used for UMS prototyping assembly. For production, design must be adapted with regard to PEB tolerances and assembly process.

The location of the RF lines is indicative and must be adjusted device by device but the same type of land pattern must be used.

DXF file available on UMS web site
http://www.ums-gaas.com

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**FOOTPRINT**

- Part number: 61 496 744
- Designation: Recommended Footprint for QFN 5x5
- Name: Belloche
- Sheet: 01 of 01
- Projection: 24/32

Subject to change without notice.
6.9. Recommended evaluation board for QFN 3x3, 16 leads
6.10. Recommended evaluation board for QFN 4x4, 24 leads
6.11. Recommended evaluation board for QFN 4x5, 24 leads
6.12. Recommended evaluation board for QFN 5x5, 28 leads
7. Glossary

SMD : Surface Mount Device
SMT : Surface Mount Techniques
QFN : Quad Flat Non-leaded
PCB : Printed Circuit Board
BOM : Bill Of Materials
Sij : Scattering Parameters
RoHS : Restriction of the use of certain Hazardous Substances
Lead-free : Part of the RoHS directive
DI : Deionised water
MMIC : Monolithic Microwave Integrated Circuit
THB : Temperature and Humidity Biased
HOTL : High Temperature Operating Life
Pb : Lead
MSL : Moisture Sensitivity Level

8. References

[1] : JEDEC MO-220. Thermally enhanced plastic very thin and very very thin fin pitch quad flat no lead package.


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