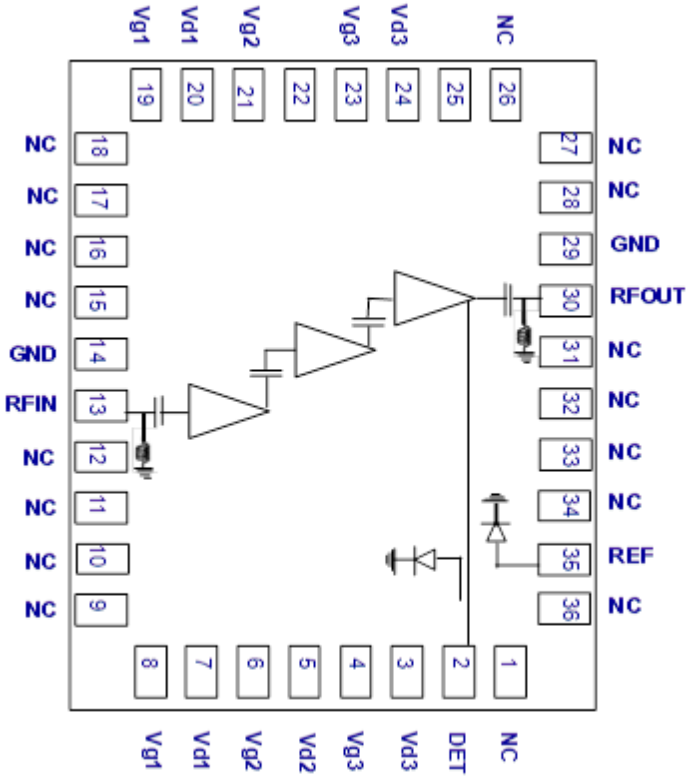
Advanced Information: AI1802

17.0-23.6GHz High Power Amplifier

GaAs Monolithic Microwave IC



The device is a High Power Amplifier monolithic circuit. It is a three stage amplifier with integrated differential mode power detector at the output. It typically exhibits a gain of 22dB, with 34dBm saturated output power for an overall DC consumption of 1.3A at 6V. Gain control up to 15dB is achievable thanks to gate voltage. On top, this circuit presents very good return loss and is fully protected against ESD.

The circuit is highly linear and compatible with the last generation of Digital Pre-Distortion.
Its versatile biasing condition helps to tune the performances. It is a field proven solution for Point to Point telecommunication systems, and also suitable for other applications such as SATCOM.

It is developed on a robust 0.15µm gate length pHEMT space evaluated process and will be available in bare die.

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17.0		23.6	GHz
Gain(1)	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat(1)	Saturated Output Power		34		dBm
OIP3	Output IP3		38		dBm
PAE	PAE at saturation		20		%
CG	Gain control range		15		dB
Rlin(1)	Input Return Loss		18		dB
Rlout(1)	Output Return Loss		20		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		10 to 1500		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		1.3		A

These values are representative of onboard measurements as defined in paragraph "Evaluation mother board".

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8V	V
Id	Drain bias quiescent current	1600	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive	+18	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	7, 20	DC Drain voltage 1st stage	6.0	V
Vd2	5, 22	DC Drain voltage 2nd stage	6.0	V
Vd3	3, 24	DC Drain voltage 3rd stage	6.0	V
Vg1	8, 19	DC Gate voltage 1st stage	-0.65	V
Vg2	6, 21	DC Gate voltage 2nd stage	-0.65	V
Vg3	4, 23	DC Gate voltage 3rd stage	-0.65	V

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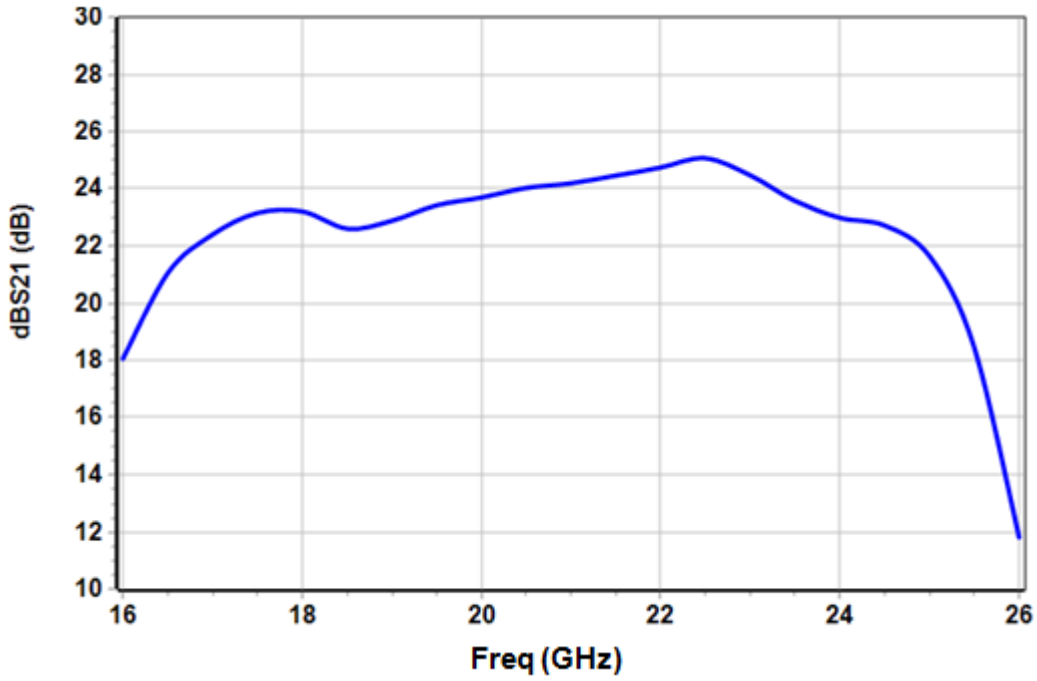
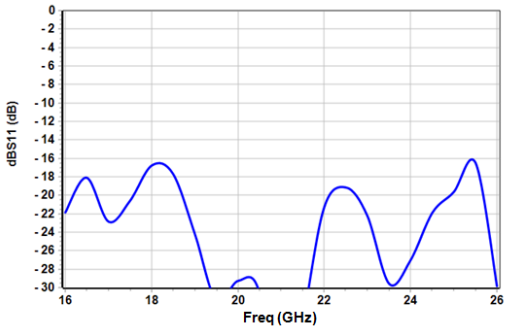
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA, Pulse width=25µs, Duty cycle =10%
Measurement performed in the access plans of the connectors, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

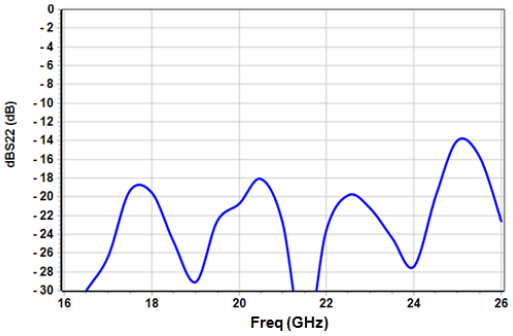
Linear Gain versus Frequency



Input Return Loss versus Frequency



Output Return Loss versus Frequency



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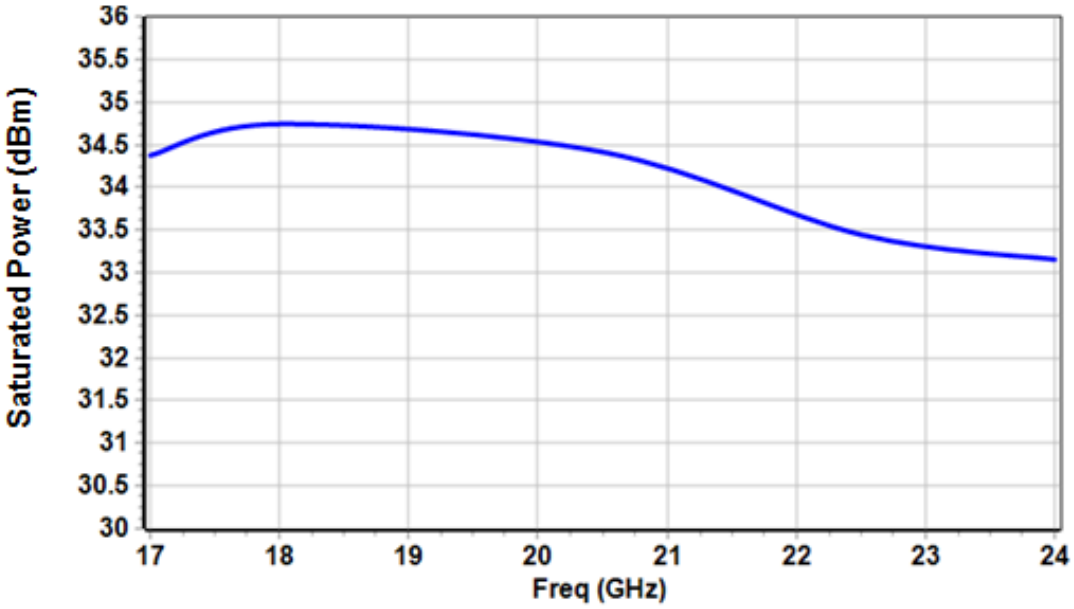
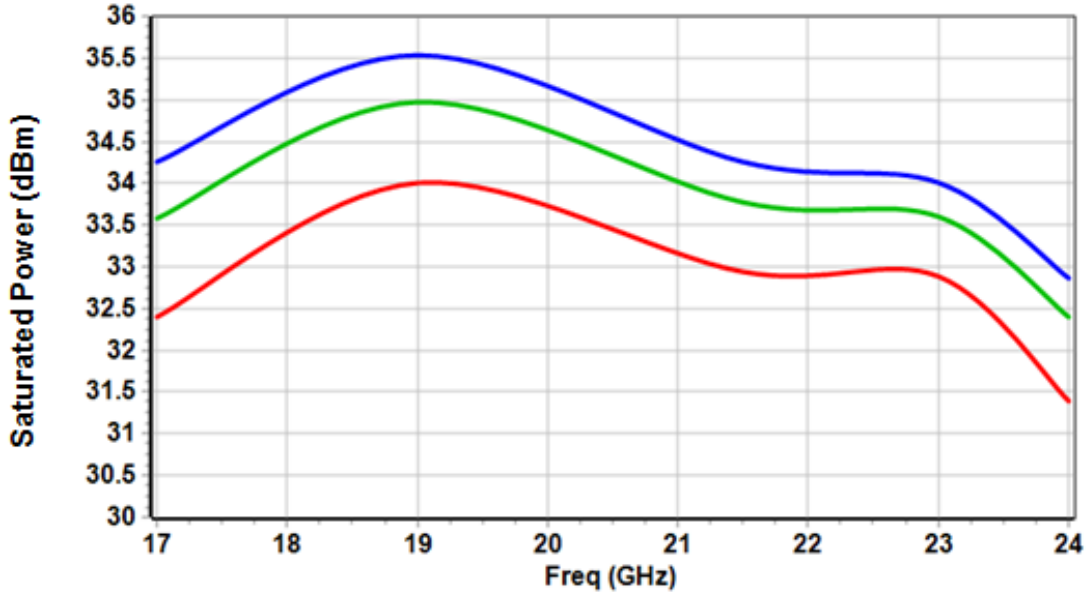
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Saturated Power versus Frequency
(in the access plans of the chip)



Saturated Power versus Frequency
(Temp.=-40 & +25 & +85 °C)



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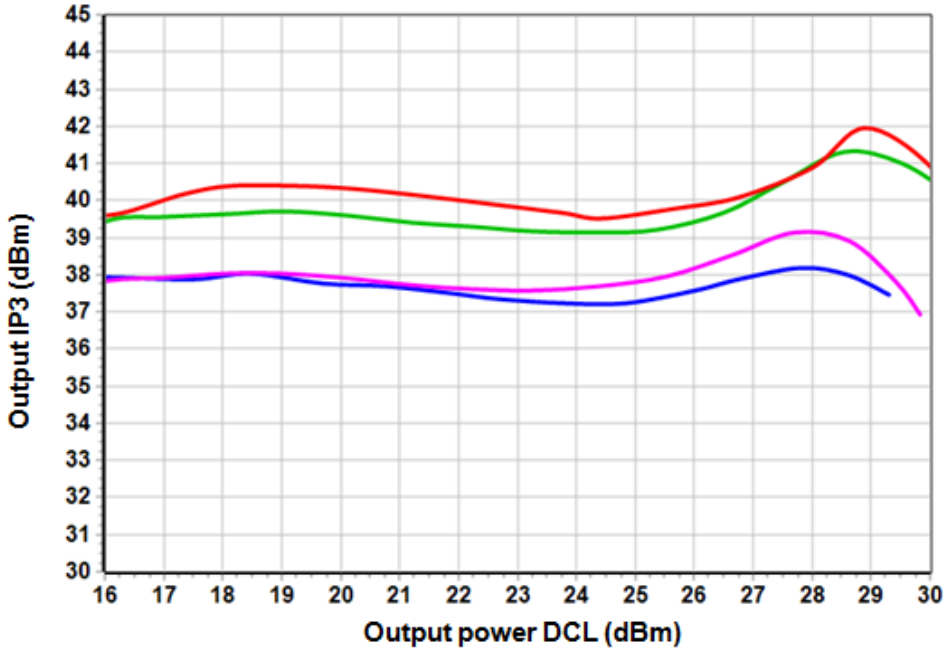
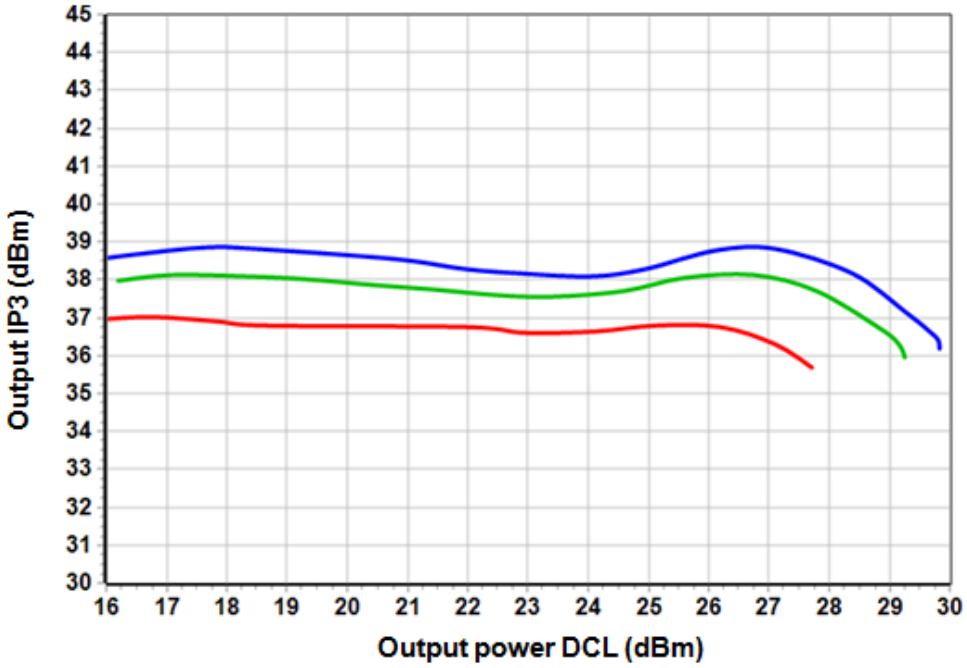
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Output IP3 versus Output Power
(Freq.=18 & 19 & 22.5 & 24 GHz)



Output IP3 versus Output Power @18GHz
(Temp.=-40 & +25 & +85 °C)



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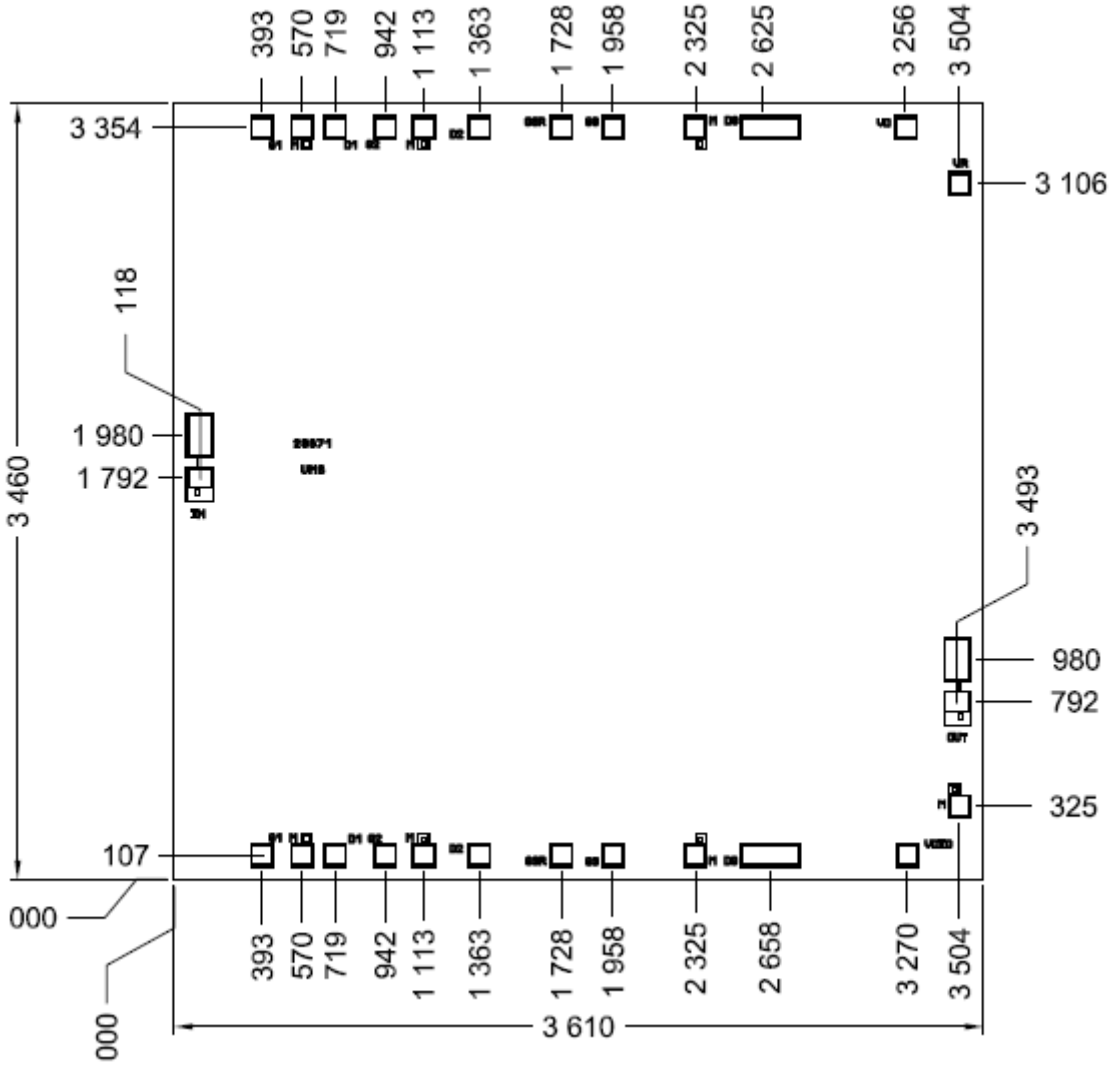
Mechanical data



Chip thickness: 100µm.
All dimensions are in micrometers

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Biasing procedure

Device Power Up instructions:

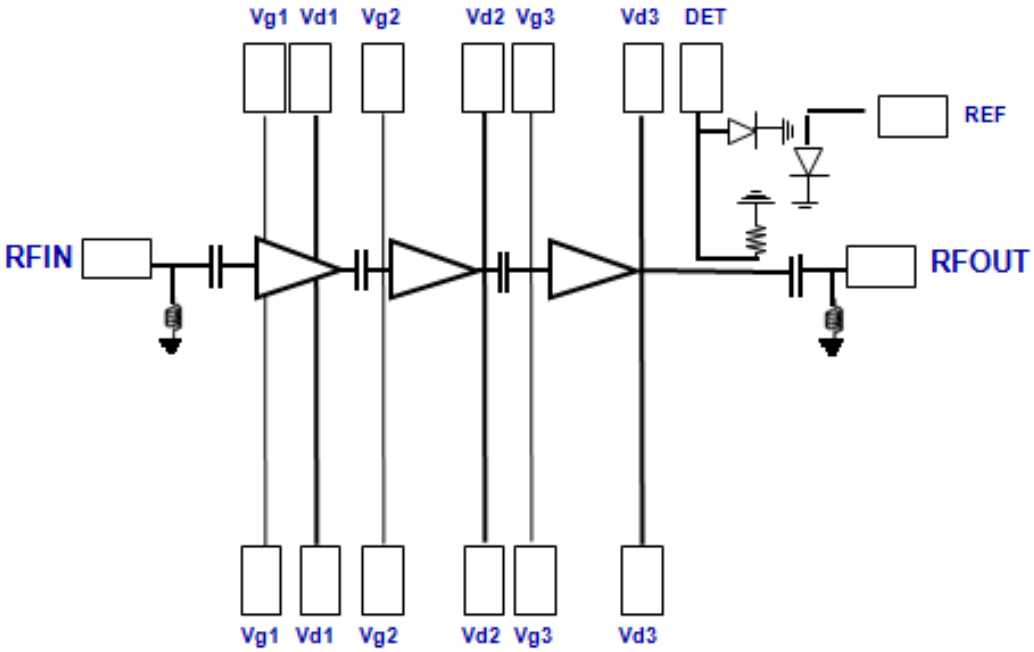
1. Ground the device
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -2V)
3. Apply Vds quiescent bias voltage (Example: Vd = 6V)
4. Increase slowly Vgs up to quiescent bias drain current Ids0 (pulsed applied on the gate)
5. Apply RF input power

Device Power down instructions:

1. Remove RF input power
2. Decrease HPA gate voltage up to Vg -2V
3. Decrease drain voltage up to 0V

Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor, therefore it is mandatory to provide a good external DC decoupling (22pF, 100pF, 10nF, 1µF) on the PC board, as close as possible to the bare die.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC accesses.

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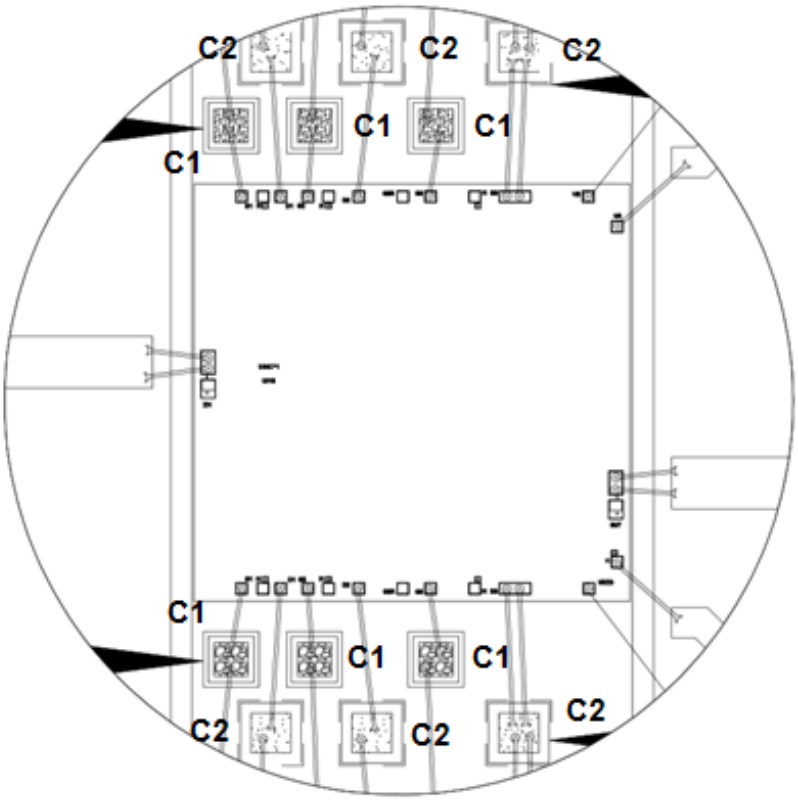
Recommended assembly plan



C1=22pF (on gate access) & C2=100pF (on drain access)

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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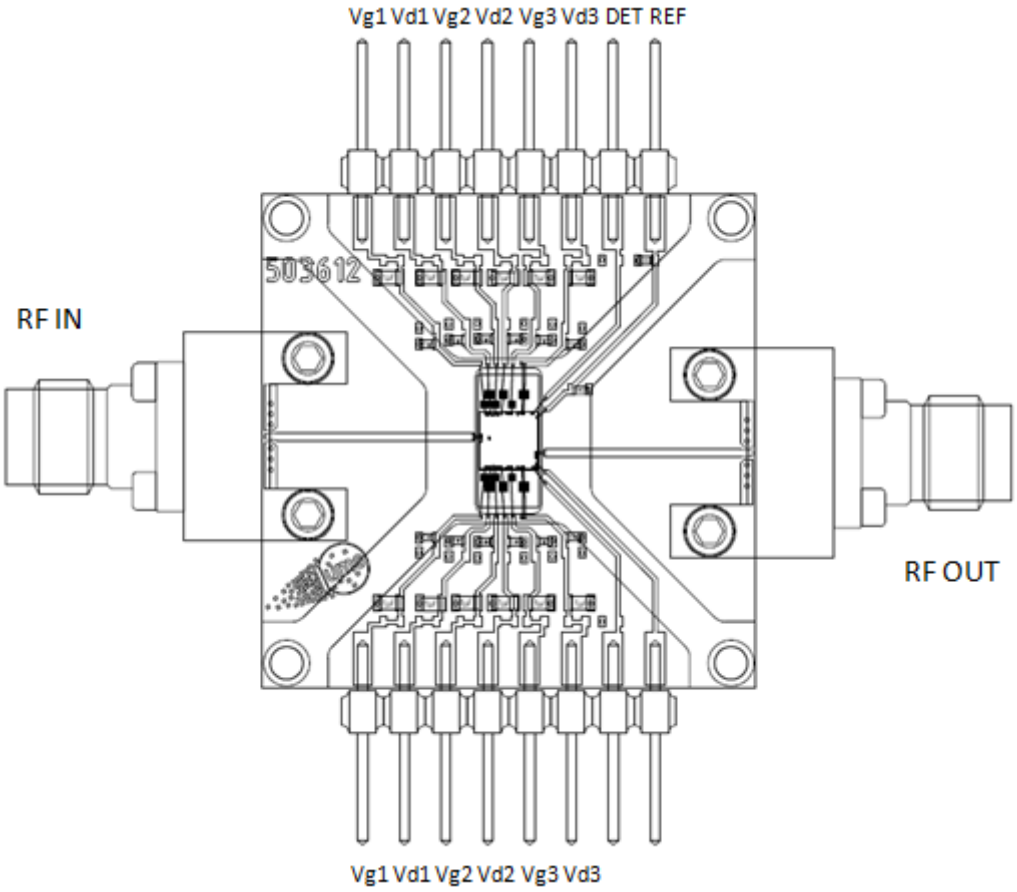
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003C / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the chip.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 22pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the gate accesses.
- Decoupling capacitors of 120pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the drain accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



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